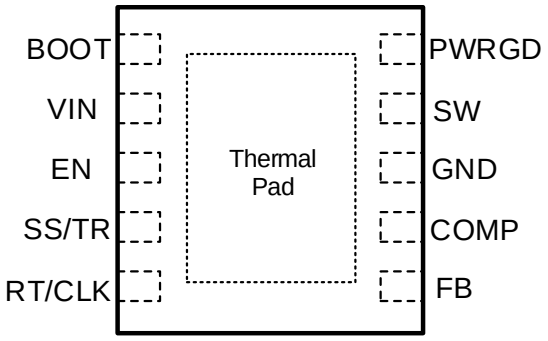
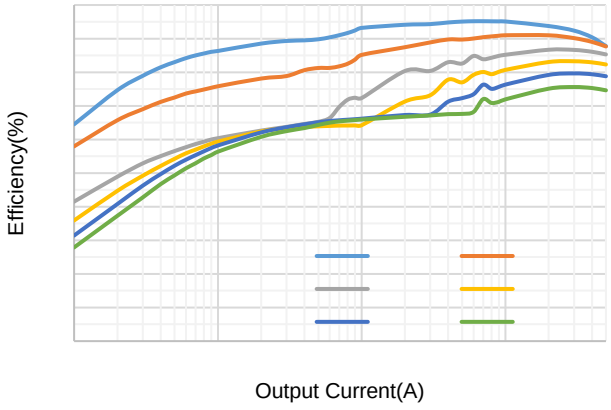
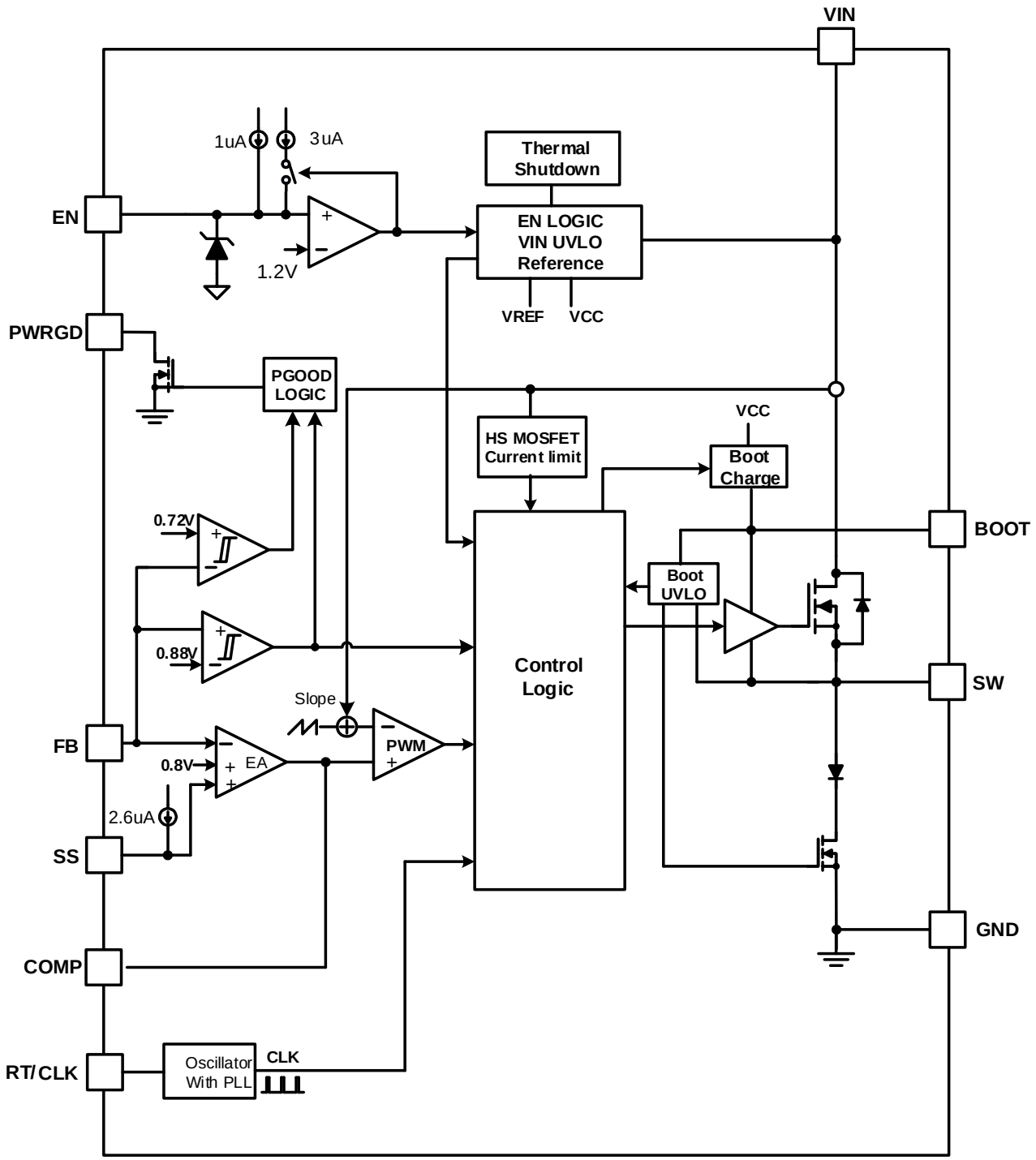

BOOT
VIN
EN
SS/TR
RT/CLK
Thermal
Pad
PWRGD
SW
GND
COMP
FB

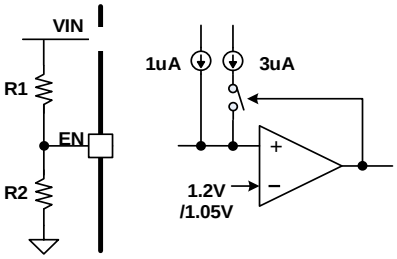
		Inverting input of the trans-conductance error amplifier. The tap of external feedback resistor divider from the output to GND sets the output voltage. The device regulates FB voltage to the internal reference value of 0.8V typical.
		An open drain output, asserts low if output voltage is low due to thermal shutdown, dropout, over-voltage or EN shut down.

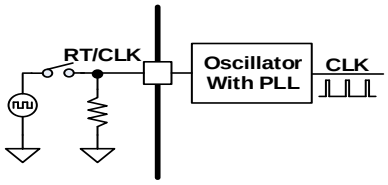
(1)
(2)

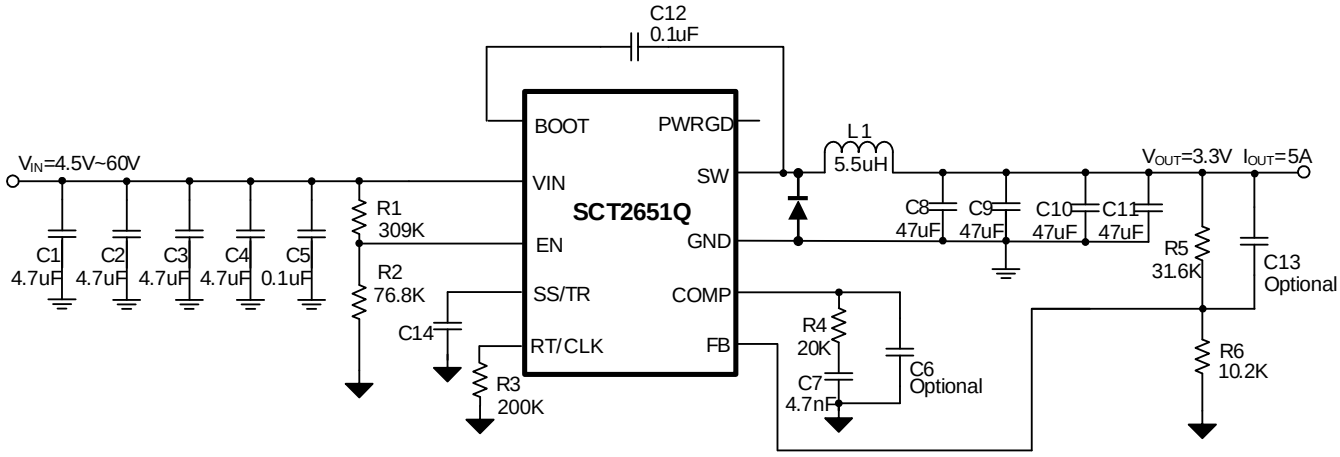
V_{UVP}	Feedback under voltage with respect to reference voltage	V_{FB}/V_{REF} rising V_{FB}/V_{REF} falling		

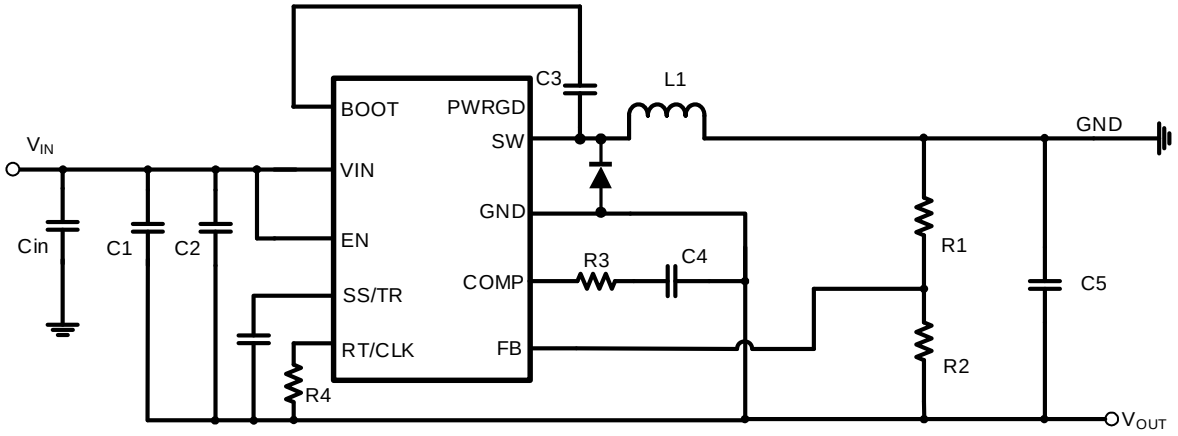

Efficiency(%)
Output Current(A)

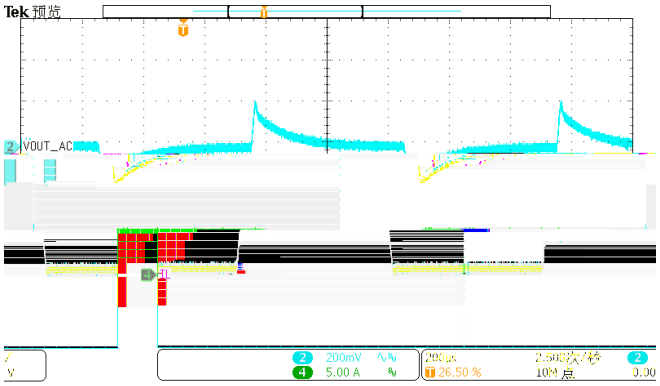

VIN
1uA
3uA
Thermal Shutdown
EN
EN LOGIC
VIN UVLO
Reference
1.2V
VREF
VCC
PWRGD
PGOOD LOGIC
VCC
HS MOSFET Current limit
Boot Charge
0.72V
BOOT
Boot UVLO
0.88V
Control Logic
SW
Slope
FB
PWM
0.8V
EA
2.6uA
SS
GND
COMP
RT/CLK
Oscillator With PLL
CLK

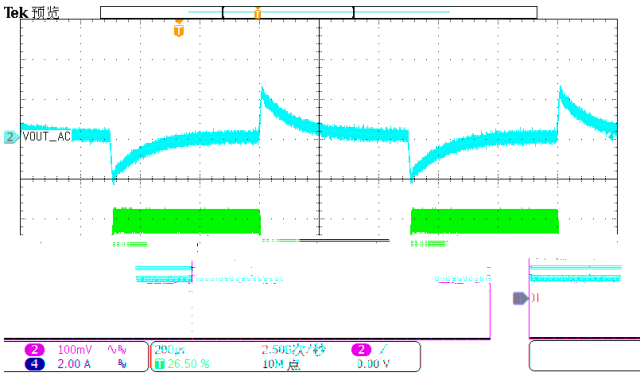

VIN
R1
EN
R2
1uA
3uA
+
−
1.2V
/1.05V

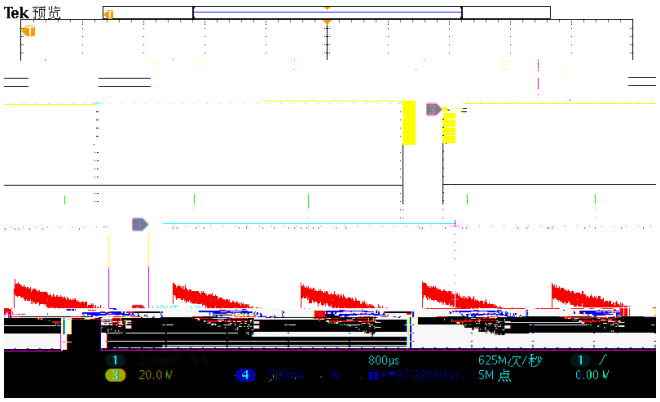

RT/CLK
Oscillator
With PLL
CLK

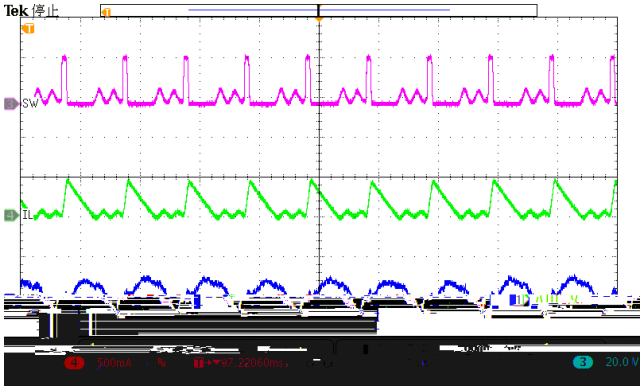

C12
0.1uF
BOOT
PWRGD
VIN
SW
SCT2651Q
EN
GND
SS/TR
COMP
RT/CLK
FB
L1
5.5uH
VIN=4.5V~60V
VOUT=3.3V
IOUT=5A
C1
4.7uF
C2
4.7uF
C3
4.7uF
C4
4.7uF
C5
0.1uF
R1
309K
R2
76.8K
C14
R3
200K
C8
47uF
C9
47uF
C10
47uF
C11
47uF
R5
31.6K
C13
Optional
R4
20K
C7
4.7nF
C6
Optional
R6
10.2K

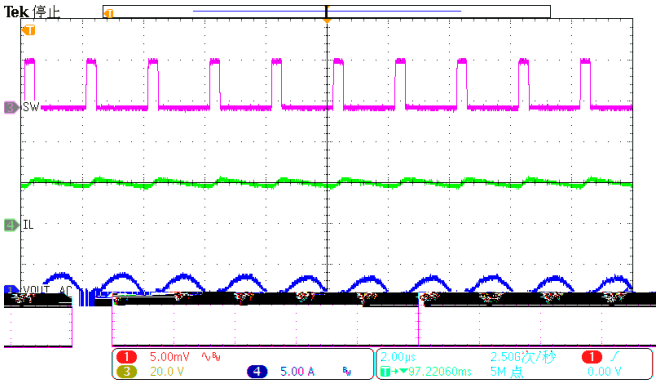

BOOT
PWRGD
SW
VIN
GND
EN
COMP
SS/TR
RT/CLK
FB
C3
L1
GND
VIN
Cin
C1
C2
R3
C4
R1
C5
R2
R4
VOUT

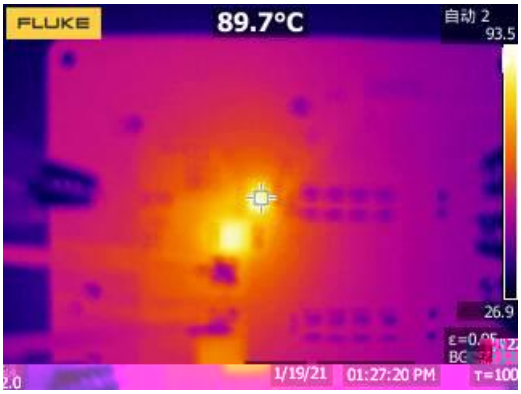

Tek 预览
VOUT_AC
200mV
5.00 A
200µs
26.50 %
2.50G次/秒
10M 点


Tek 预览
VOUT_AC
100mV
2.00 A
200µs
26.50 %
2.50G次/秒
10M 点
0.00 V

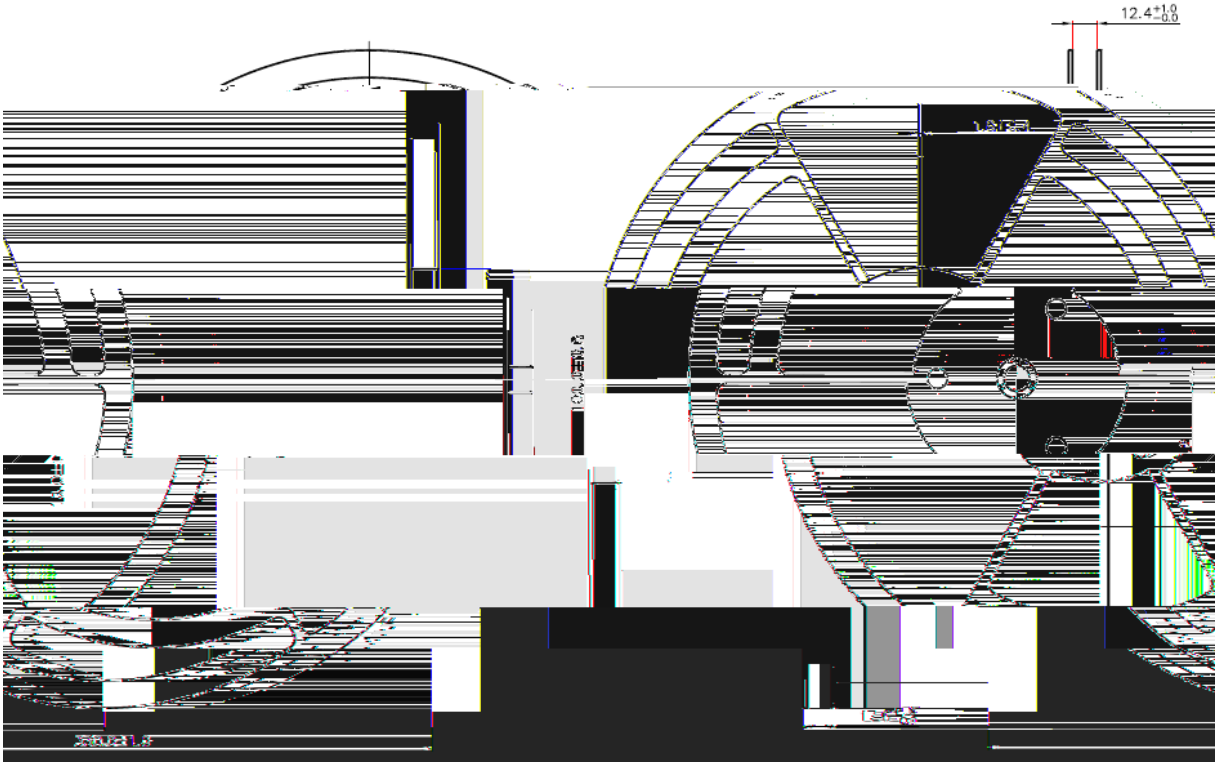

Tek 预览
800µs
625M次/秒
5M 点
20.0 V
0.00 V

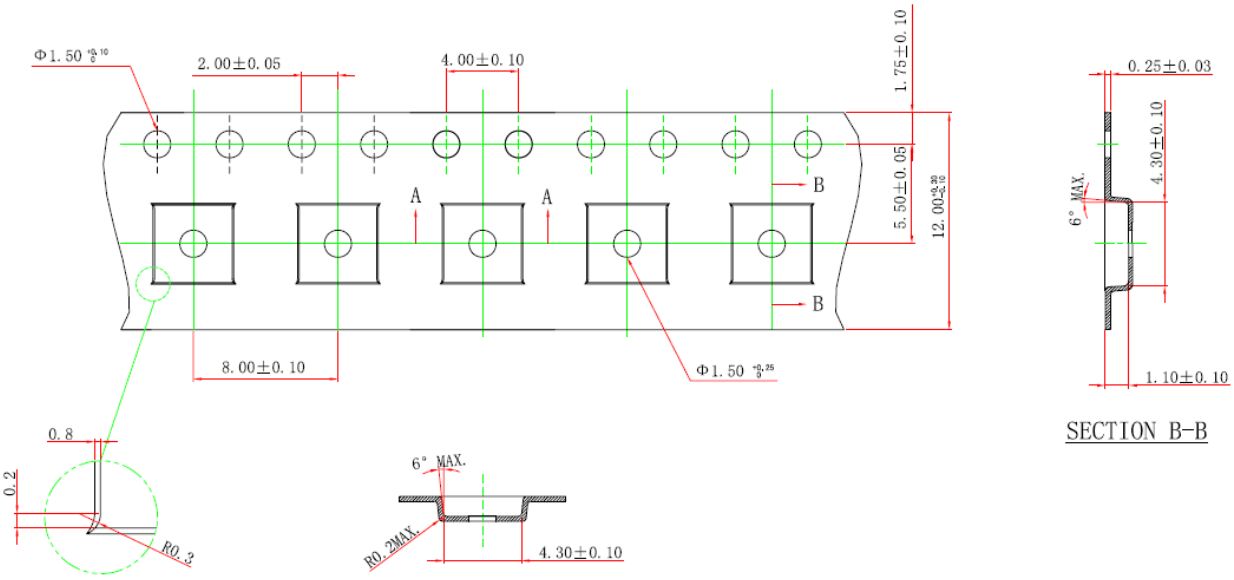

Tek 停止
SW
IL
20.0 V


Tek 停止
SW
IL
VOUT_AC
5.00mV
20.0 V
5.00 A
2.00µs
2.50G次/秒
5M 点
0.00 V


FLUKE
89.7°C
自动 2
93.5
26.9
1/19/21
01:27:20 PM

1.


12.4 +1.0 -0.0


Φ1.50 +0.10 0
2.00±0.05
4.00±0.10
1.75±0.10
5.50±0.05
12.00 +0.20 -0.10
A
A
B
B
8.00±0.10
Φ1.50 +0.25 0
0.8
0.2
R0.3
6° MAX.
R0.2MAX.
4.30±0.10
0.25±0.03
4.30±0.10
6° MAX.
1.10±0.10
SECTION B-B