NOTE: Page numbers for previous revisions may differ from page numbers in the current version.
Revision 1.0: Production
Revision 1.1: Update DEVICE ORDER INFORMATION

ORDERABLE DEVICE	PACKAGING TYPE	STANDARD PACK QTY	PACKAGE MARKING	PINS	PACKAGE DESCRIPTION
SCT63240AFIAR	Tape & Reel	5000	240A	19	QFN-19L

Over operating free-air temperature unless otherwise noted(1)

DESCRIPTION	MIN	MAX	UNIT
VIN	-0.3	24	V
PVIN1, PVIN2	-0.3	20	V
SW1,SW2	-1	20	V
SW3	-1	24	V
BST1,BST2	-0.3	26	V
BST3	-0.3	30	V
BST1-SW1,BST2-SW2,BST3-SW3	-0.3	6	V
VDD, V3P3, VREF, ISNS, EN, PWM1, PWM2 EMC /Spar			

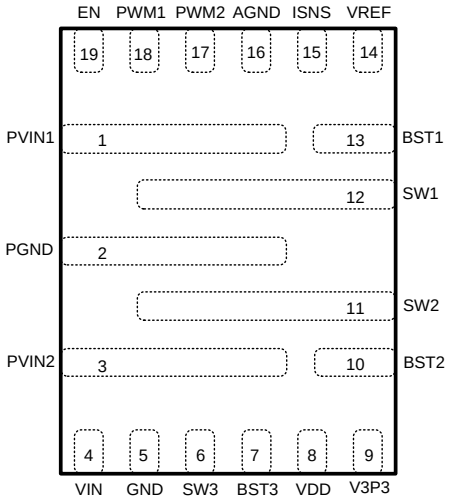


Figure 1. Top view 19-Lead QFN 3mm*4mm

© 2022 Silicon Content Technology Co., Ltd. All Rights Reserved

4	Input supply voltage of the Buck converter. Add a local bypass capacitor from VIN pin to GND pin. Path from VIN pin to high frequency bypass capacitor and GND must be as short as possible.
5	Power ground of the Buck converter.
6	Switching output of the Buck converter. Connect SW3 to an external power inductor.
7	Power supply bias for the high-side power MOSFET gate driver of Buck converter. Connect a 0.1uF capacitor from BST3 pin to SW3 pin.
8	Output voltage of the Buck converter. Connect 22uF capacitor from this pin to GND pin. VDD is also the input power supply for gate driver of power stage, the 3.3V LDO and the 2.5V voltage reference.
9	3.3V LDO output. Connect 1uF capacitor to ground.
10	Power supply bias for the high-side power MOSFET gate driver of Q3 as shown in the block diagram. Connect a 0.1uF capacitor from BST2 pin to SW2 pin.
11	Switching node of the half-bridge FETs Q3 and Q4.
12	Switching node of the half-bridge FETs Q1 and Q2.

PARAMETER	THERMAL METRIC	DFN-19L	UNIT
R	Junction to ambient thermal resistance(1)	42	°C/W
R	Junction to case thermal resistance(1)	45	

(1) SCT provides R and R numbers only as reference to estimate junction temperatures of the devices. R and R are not a characteristic of package itself, but of many other system level characteristics such as the design and layout of the printed circuit board (PCB) on which the SCT63240A is mounted, thermal pad size, and external environmental factors. The PCB board is a heat sink that is soldered to the leads of the SCT63240A. Changing the design or configuration of the PCB board changes the efficiency of the heat sink and therefore the actual R and R .

V_{IN}=V_{PVIN1}=V_{PIN2}=12V, VDD=5V, typical value is tested under 25°C.

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
Input supplies and UVLO						
V_{IN}	Operating input voltage		4.2		20	V
P_{VIN}	Operating input voltage		1		17	V
V_{IN_UVLO}	V_{IN} UVLO Threshold	V_{IN} rising		3.6		V
	Hysteresis			400		mV
V_{DD_UVLO}	V_{DD} UVLO Threshold	V_{DD} rising		3.8		V
	Hysteresis			440		mV
I_{SHDN}	Shutdown current from VIN pin	EN=0V, VIN=12V		1	3	

© 2022 Silicon Content Technology Co., Ltd. All Rights Reserved

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
F_{SW}	Switching frequency		540	600	660	KHz
V_{DD}	Output voltage		4.925	5	5.075	V
I_{LIM_HS}	High-side power MOSFET peak current limit threshold			1.5		A
T_{HIC_W}	Over current protection hiccup wait time			0.85		ms
T_{HIC_R}	Over current protection hiccup restart time			27		ms
R_{DSON_H}	High side FET on-resistance			390		
R_{DSON_L}	Low side FET on-resistance			225		
T_{SS}	Internal soft-start time			2		ms
3.3V LDO						
V_{3P3}	Output voltage	Cout=1uF, VDD=5V	3.267	3.3	3.333	V
I_{3P3}	Output current Capability		200	285		mA
I_{SC1}	Short current			65		mA
2.5V REFFERENCE OUTPUT						
V_{2P5}	Output voltage reference	Cout=1uF, VDD=5V	2.475	2.5	2.525	V
I_{3P3}	Output current Capability		100	150		mA
I_{SC2}	Short current			60		mA
Current Sense						
V_{ISNS0}	Voltage with no input current	I_{PGND}=0A ,Tj=25 PWM1=PWM2=0V	0.55	0.6	0.65	V
R_{ISNS}	Input current to output voltage gain	$V_{ISNS}=V_{ISNS0}+I_{PGND}*R_{ISNS}$	0.98	1	1.02	V/A
Protection						
T_{SD}	Thermal shutdown threshold Hysteresis	T_J rising		155 35		°C °C

© 2022 Silicon Content Technology Co., Ltd. All Rights Reserved

Figure 2. Transfer Efficiency with 5W RX@ Vout=5V

Figure 3. Transfer Efficiency with 10W RX@ Vout=9V

Figure 4.

© 2022 Silicon Content Technology Co., Ltd. All Rights Reserved

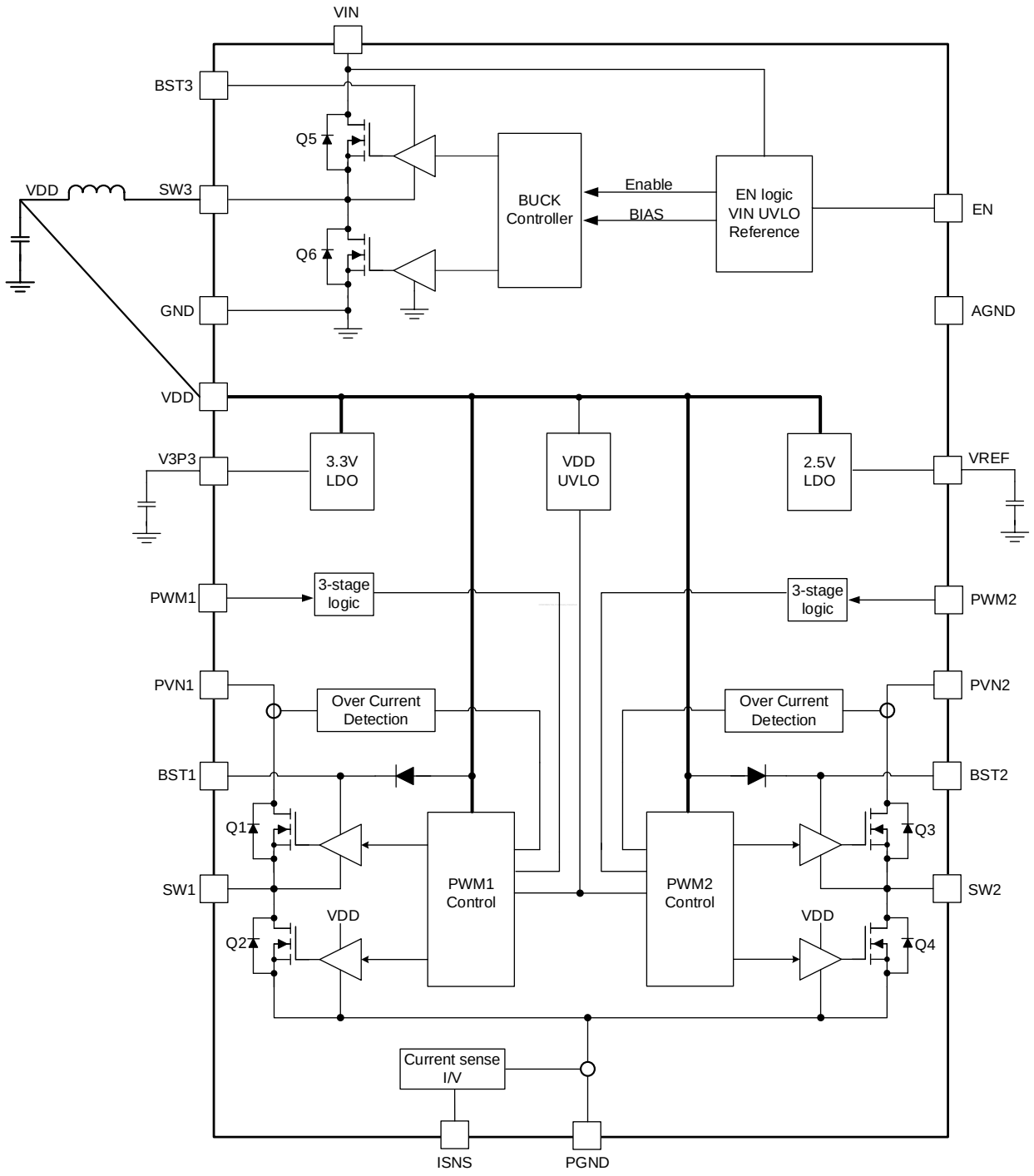


Figure 8. Functional Block Diagram

© 2022 Silicon Content Technology Co., Ltd. All Rights Reserved

Overview

The SCT63240A is a highly integrated power management unit optimized for wireless power transmitter applications. This device integrates the power functions required to a wireless power transmitter including 5V buck converter as power supply for external transmitter controller and internal 5V power supply to increase system efficiency, full bridge power stage to convert DC input power to AC output for driving LC resonant circuit, lossless current sensing with ±2% accuracy, 3.3V output LDO for powering MCU and a 2.5V reference voltage.

The SCT63240A has four power input pins. VIN is connected to the power FETs of buck converter. PVIN1 and PVIN2 are connected to the power FETs of the full bridge and conducts high currents for power transfer. VDD is the output feedback pin of the 5V output buck converter and at the mean while as the power supply for internal two LDOs and full bridge MOSFET's gate driver.

VIN and PVIN1, PVIN2 can be powered separately for more flexibility of system power design. The operating voltage range for VIN is from 4.2V to 20V. An Under-voltage Lockout(UVLO) circuit monitors the voltage of VIN pin and disable the IC operation when VIN voltage falls below the UVLO threshold of 3.2V typically. The maximum operating voltage for PVIN is up to 17V while the minimum voltage accepted can be down to 1V. Another UVLO circuit also supervise the VDD voltage which is the power supply for gate drivers of full bridge MOSFETs. Full bridge will work when VDD UVLO release.

Two independent PWM signals control two separate half bridge MOSFETs with internal adaptive non-overlap circuitry to prevent the shoot-through of MOSFETs in each bridge. PWM logics are compatible for both 3.3V and 5V IOs so the SCT63240A can accept PWM signal from the controller with using either 3.3V or 5V power supply.

The buck converter and full bridge of power MOSFETs includes proprietary designed gate driver scheme to resist switching node ringing without sacrificing MOSFET turn-on and turn-off time, which further erases high frequency radiation EMI noise caused by the MOSFETs hard switching. This allows the user to reduce the system cost and design effort for EMI reduction.

The SCT63240A full protection features include VIN and VDD under-voltage lockout, over current protection with cycle-by-cycle current limit and hiccup mode, output hard short protection for buck converter and 4-MOSFETs full bridge, current limit and current fold back at hard short for two LDOs and whole chip thermal shutdown protection.

Enable and Start up Sequence

When the VIN pin voltage rises above 3.6V and the EN pin voltage exceeds the enable threshold of 1.18V, the buck converter and two LDOs enable at once. And the device disables when the VIN pin voltage falls below 3.2V or when the EN pin voltage is below 1.1V. VDD ramp up after buck converter works, and also the V3V and VREF output do. Once VDD rise up to 3.8V and V3V is higher than 3V, 4-MOSFETs full bridge allows PWM signal to control for switching. PWM input cannot control full bridge of MOSFETs if VDD drop to 3.36V or V3V drop to 2.7V.

An internal 1.5uA pull up current source to EN pin allows the device enable when EN pin is floating to simply the system design. If an application requires a higher system under voltage lockout threshold, two external resistors divider (R1 and R2) in Figure 9 can be used to achieve an expected system UVLO. The UVLO rising and falling threshold can be calculated by Equation 1 and Equation 2 respectively.

— (

© 2022 Silicon Content Technology Co., Ltd. All Rights Reserved

5V Output Buck Converter

The SCT63240A fully integrates synchronous buck converter with up to 20V input voltage and 5V fixed output voltage, which offers up to 1A output current capability. The device employs 600KHz fixed frequency peak current mode control with the internal loop compensation network and built-in 2ms soft-start which makes this buck converter easily to be used by minimizing the off-chip component count. Pulse Skipping Modulation(PSM) is adopted to improve the light load efficiency.

The buck converter's output, a fixed 5V voltage, supports the power requirement on system such as transmitter controller or mechanical fan meanwhile it is also the power supply of the SCT63240A's 3.3V LDO, VREF LDO and gate drivers of 4-MOSFETs full bridge. Connect 22uF capacitor from VDD to GND and add a 0.1uF local bypass ceramic capacitor placed close to the IC.

The converter has proprietary designed gate driver scheme to resist switching node ringing without sacrificing MOSFET turn-on and turn-off time, which further erases high frequency radiation EMI noise caused by the MOSFETs hard switching.

An external 100nF ceramic bootstrap capacitor between BST3 and SW3 pin powers floating high-side power MOSFET gate driver. The bootstrap capacitor voltage is charged from an integrated voltage regulator when high-side power MOSFET is off and low-side power MOSFET is on.

Buck converter implements over current protection with cycle-by-cycle limiting high-side MOSFET peak current and also low-side MOSFET valley current to avoid inductor current running away during unexpected overload and hiccup protection in output hard short condition. When overload or hard short happens, the converter cannot provide output current to satisfy loading requirement even though the inductor current has already been clamped at over current limitation. Thus, output voltage drops below regulated voltage continuously. When output voltage under regulation lasts for 850 us, the converter stops switching; After remaining OFF for 13.6 ms the device will attempt to restart from soft-start.

The hiccup protection mode above greatly reduces the average short circuit current to alleviate thermal issues and protect the regulator.

Full bridge and PWM Control

The SCT63240A integrate full bridge power stage with only 15mohm on-resistance for each power MOSFET optimized for wireless power transmitter driving the LC resonant circuit. This full bridge is able to operate in a wide switching frequency range from 20KHz to 400KHz for different applications which is completely compatible with WPC's frequency requirement from 100KHz to 205KHz.

PWM1 input controls the half bridge comprised of high side MOSFET Q1 and low side MOSFET Q2, and PWM2 input controls the half bridge comprised of high side MOSFET Q3 and low side MOSFET Q4 as shown in block diagram. The PWM1 and PWM2 independently control the SW1 and SW2 duty cycle and frequency. Logic HIGH will turn off low side FET and turn on high side FET, and logic LOW will turn off high side FET and turn on low side FET.

PWM1 and PWM2 also support tri-state input. When PWM input logic first enters tri-state either from logic HIGH or logic LOW, the states of its controlled FETs stay the same. If the PWM input stays in the tri-state for more than 60ns, its controlled FETs are all turned off, and the corresponding SW output becomes high impedance. The FETs stay off until the PWM logic reaches logic HIGH or logic LOW threshold.

An external 100nF ceramic bootstrap capacitor between BST1 and SW1 pin powers floating high-side power MOSFET Q1's gate driver, and the other 100nF bootstrap capacitor between BST2 and SW2 pin powers for the Q3's. When low side FET is on which means SW is low, the bootstrap capacitor is charged through internal path by VDD power supply rail.

PWM cannot been kept as high level for more than 2ms since the voltage of bootstrap capacitor will be discharged by internal leakage current if high side FET keeps on.

© 2022 Silicon Content Technology Co., Ltd. All Rights Reserved

Typical Application

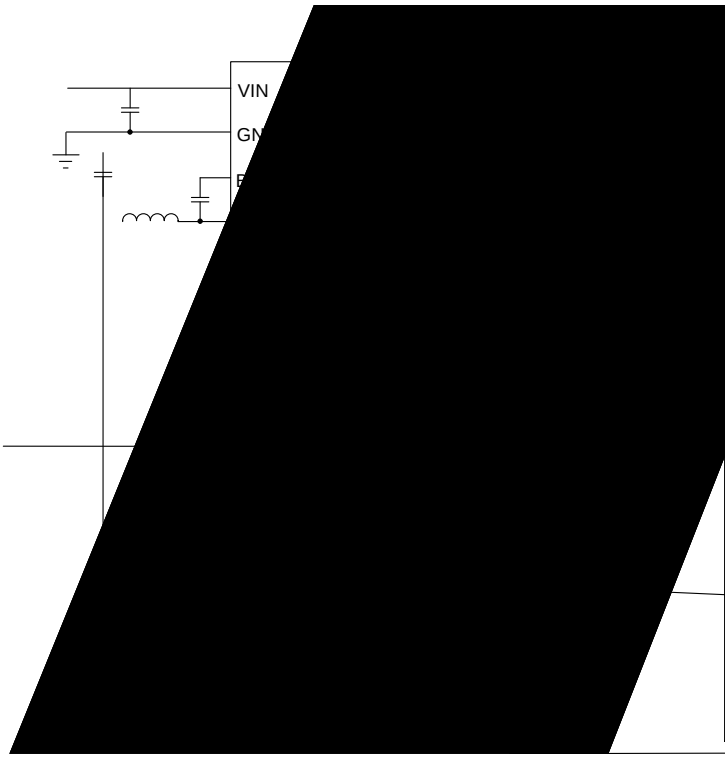


Figure 10. Same Input to VIN and PVIN

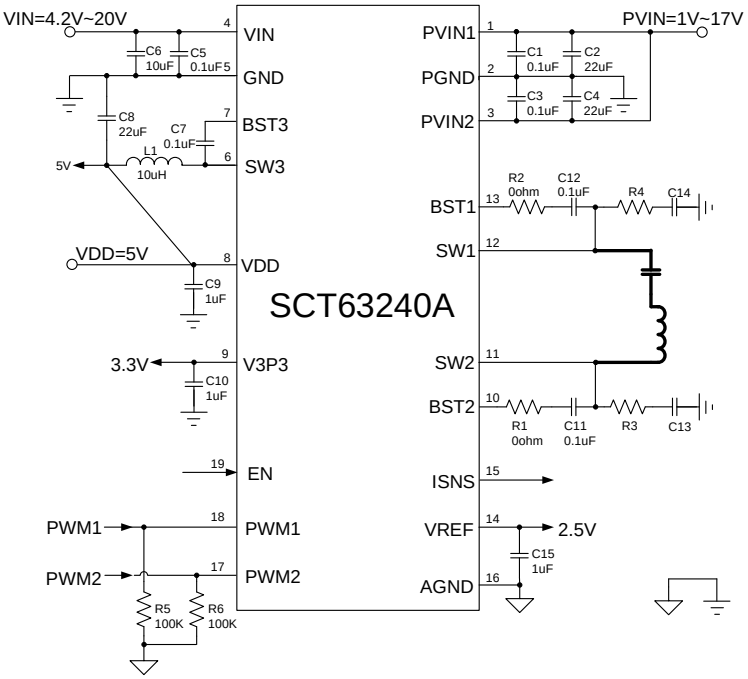


Figure 11. Separate Input to VIN and PVIN

© 2022 Silicon Content Technology Co., Ltd. All Rights Reserved

Application Waveforms

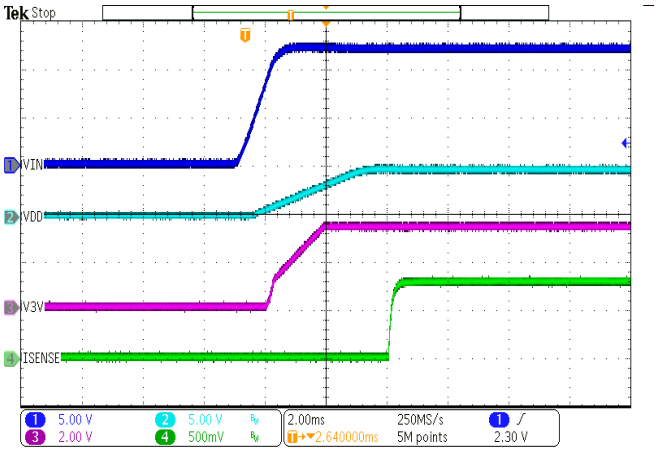


Figure 12. Power Up

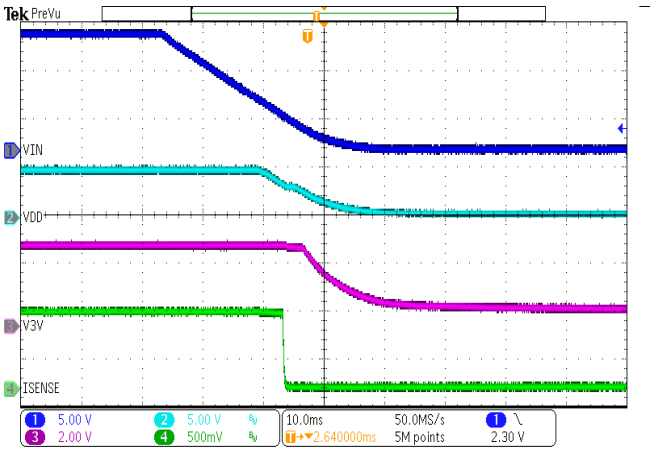


Figure 13. Power Down

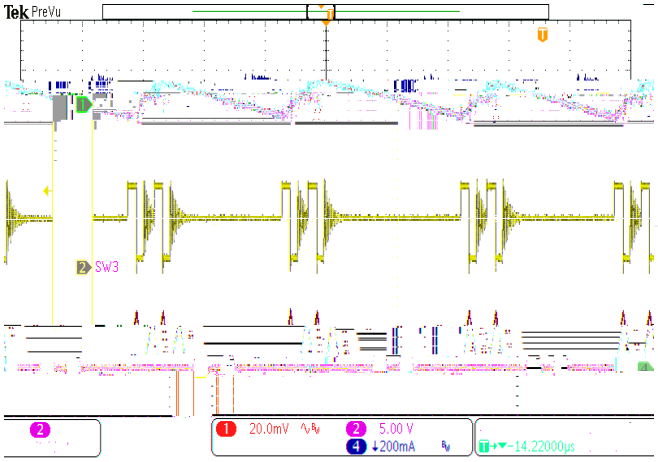


Figure 14. VDD Ripple and SW3 @VIN=9V, IOUT=20mA

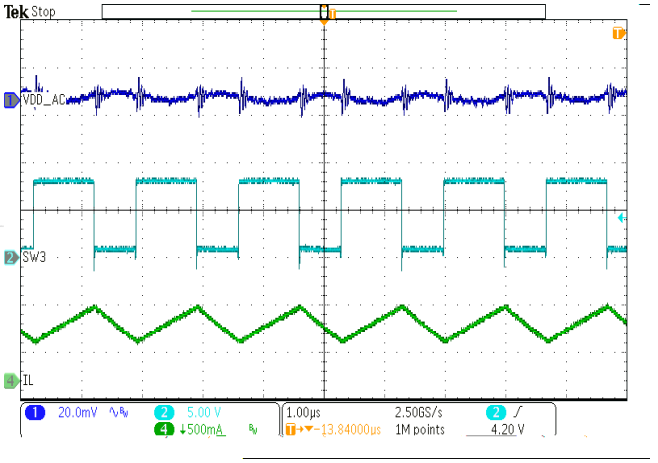


Figure 15. VDD Ripple and SW3 @VIN=9V, IOUT=600mA

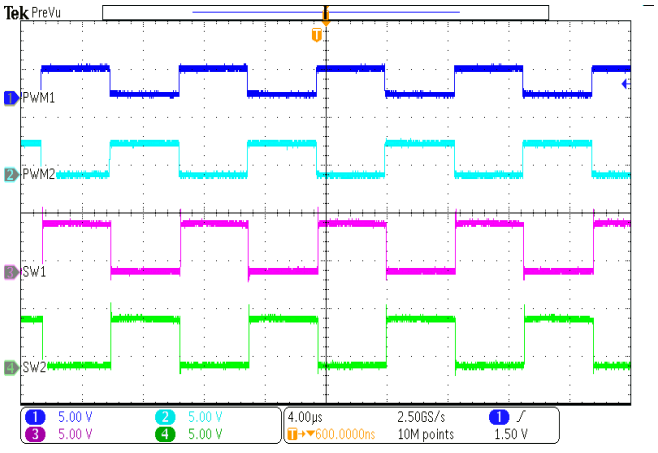


Figure 16. Full bridge @Vin=5V, RX=5W

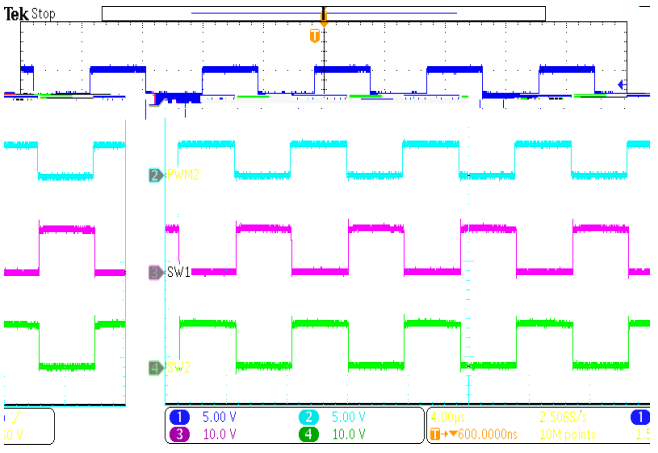


Figure 17. Full bridge @Vin=9V, RX=10W

© 2022 Silicon Content Technology Co., Ltd. All Rights Reserved

Layout Guideline

Proper PCB layout is a critical for SCT63240A
switching currents or voltages are easy to interact with stray inductance and parasitic capacitance to generate noise and degrade performance. For better results, follow these guidelines as below:

1. Bypass capacitors from PVIN to PGND should put next to PVIN and PGND pin as close as possible especially for the two small capacitors.
2. PGND connect to bottom layer by via between capacitors.
3. Bypass capacitors from VIN to GND should put next to VIN and GND pin as close as possible especially for the small capacitor.
4. Buck converter output capacitor's ground should connect to GND directly to minimize the power loop.
5. VDD pin can connect to the DC/DC's output capacitor from bottom layer, connect to the point behind the capacitor while not connect to inductor.
6. Bypass capacitor for VDD place next to VDD pin.
7. Bypass capacitor for V3P3 place next to V3P3 pin.
8. Bypass capacitor for VREF place next to VREF pin.
9. AGND pin connect to common ground by Kelvin connection.

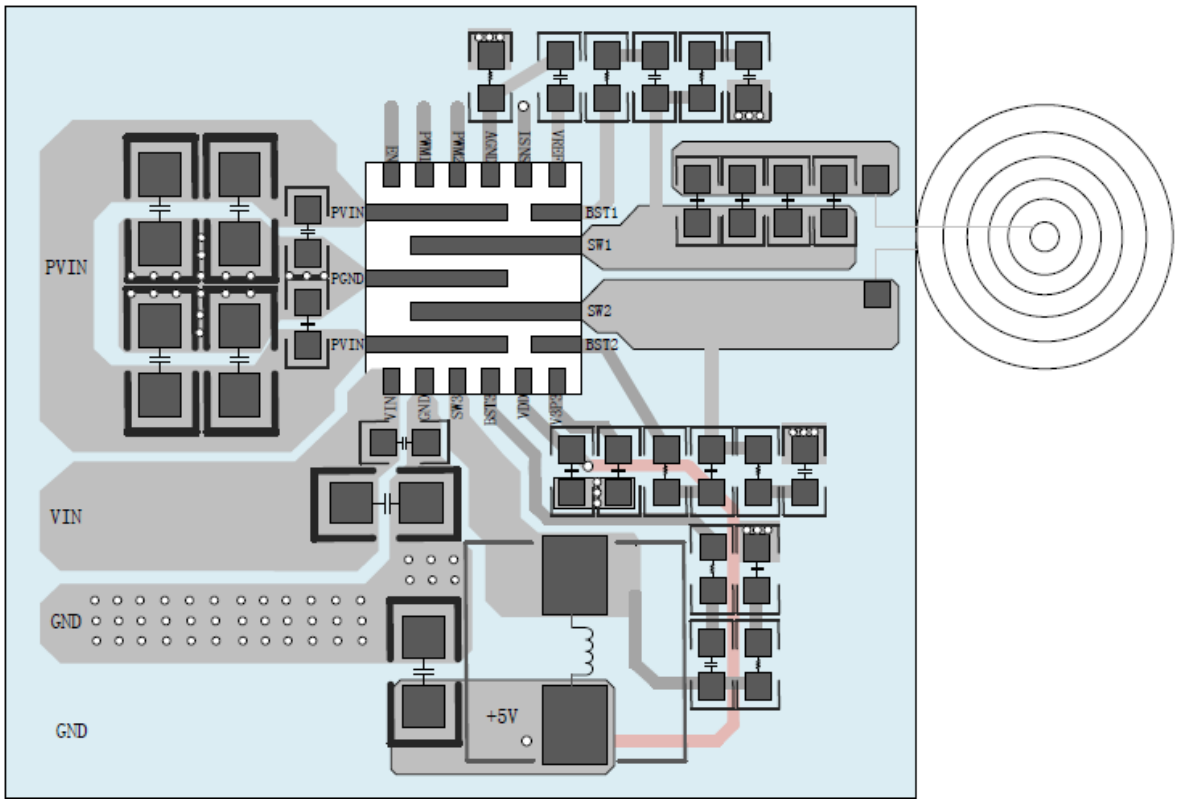
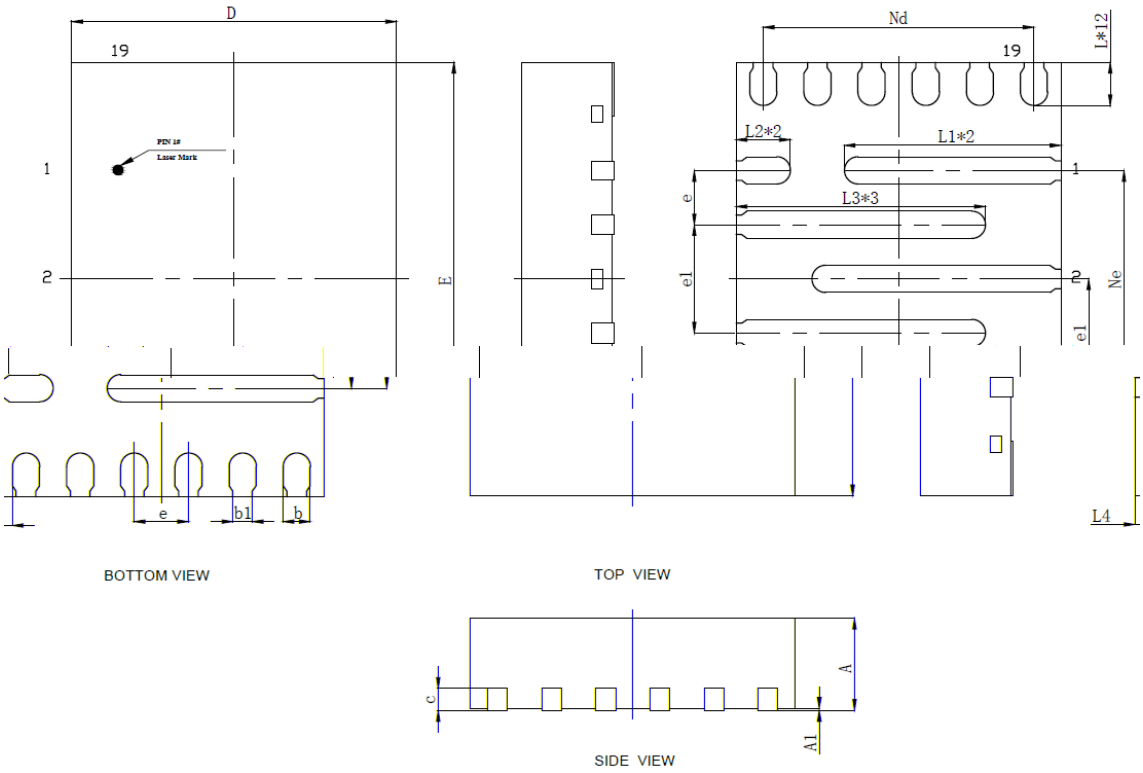


Figure 24. PCB Layout Example

© 2022 Silicon Content Technology Co., Ltd. All Rights Reserved



FCQFN-19L (3x4) Package Outline Dimensions

Symbol	Dimensions in Millimeters		
	Min.	Nom.	Max.
A	0.80	0.85	0.90
A1	0	0.02	0.05
b	0.20	0.25	0.30
b1		0.18 REF	
c		0.203 REF	
D	2.90	3.00	3.10
Nd		2.50 BSC	
Ne		2.00 BSC	
e		0.50 BSC	
e1		1.00 BSC	
E	3.90	4.00	4.10
L	0.35	0.40	0.45
L1	1.95	2.00	2.05
L2	0.45	0.50	0.55
L3	2.25	2.30	2.35
L4	0.075	0.125	0.175

NOTE:

1. Drawing proposed to be made a JEDEC package outline MO-220 variation.
2. Drawing not to scale.
3. All linear dimensions are in millimeters.
4. Thermal pad shall be soldered on the board.
5. Dimensions of exposed pad on bottom of package do not include mold flash.
6. Contact PCB board fabrication for minimum solder mask web tolerances between the pins.

© 2022 Silicon Content Technology Co., Ltd. All Rights Reserved

DIMENSIONS

	C	D	t
	Ø100±1	Ø13.3±0.3	2.0±0.3

DIMENSIONS

	B0 (mm)	K0 (mm)	t (mm)	P (mm)
	4.40±0.10	1.14±0.10	0.25±0.02	8±0.10

	D (mm)	D1 (mm)	P0 (mm)	10P0 (mm)

© 2022 Silicon Content Technology Co., Ltd. All Rights Reserved