3.5V-36V Vin, 6A, High Efficiency Synchronous Step-down DCDC Converter

Features

- Wide Input Range: 3.5V-36V
- Up to 6A Continuous Output Current
- 1V ±1.5% Feedback Reference Voltage
- Integrated 30 -Side and 18 Low-Side Power MOSFETs
- 13uA Quiescent Current with VBIAS Connected to an auxiliary power supply to 5V
- 60ns Minimum On-time
- 4ms Internal Soft-start Time
- Adjustable Frequency 200KHz to 1.8MHz
- External Clock Synchronization
- Frequency Spread Spectrum (FSS) Modulation for EMI Reduction
- External bias option for improved efficiency
- Precision Enable Threshold for adjustable Input Voltage Under-Voltage Lock Out Protection (UVLO) Threshold and Hysteresis
- Parallel input path to minimize switch node ringing
- Low Dropout Mode Operation
- Over-voltage and Over-Temperature Protection
- Available in 3.5mm*4mm QFN-14L Package

Applications

- Automotive infotainment and ADAS
- USB Type-C Power Delivery, USB Charging
- Industrial and Medical Distributed Power Supplies

General Description

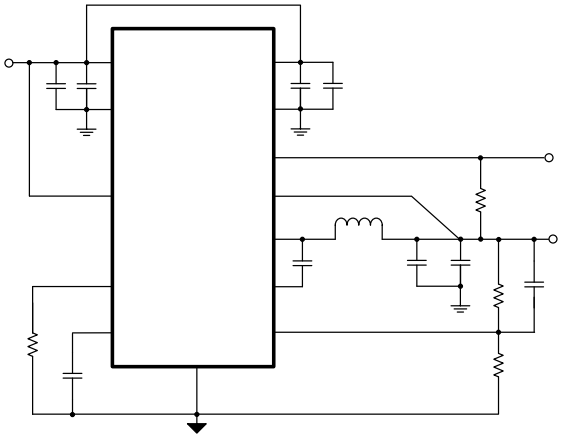
The SCT2464 is 6A synchronous buck converters with wide input voltage, ranging from 3.5V to 36V, which integrates a 30 high-side MOSFET and a 18 low-side MOSFET. The SCT2464, adopting the peak current mode control, supports the Pulse Skipping Modulation (PSM) with typical 13uA (VBIAS=5V) low quiescent current which assists the converter on achieving high efficiency at light load or standby condition.

The SCT2464 features adjustable switching frequency from 200kHz to 1.8MHz with an external resistor, which provides the flexibility to optimize either efficiency or external component size. The converter supports external clock synchronization with a frequency band from 200kHz to 1.8MHz. The SCT2464 allows power conversion from high input voltage to low output voltage with a minimum 60ns on-time of high-side MOSFET.

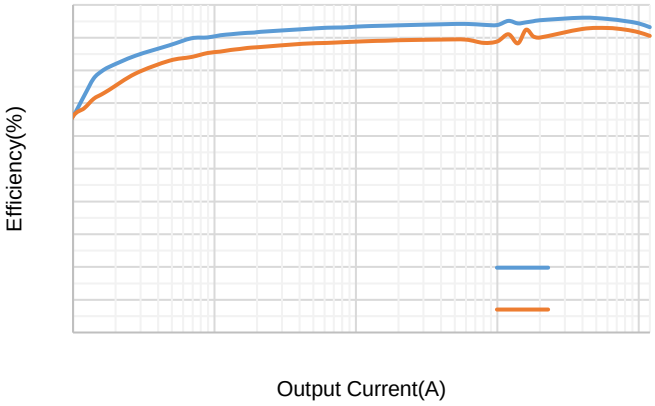
The SCT2464 is an Electromagnetic Interference (EMI) friendly buck converter with implementing optimized design for EMI reduction. The SCT2464 features Frequency Spread Spectrum FSS with ±6% jittering span of the 500kHz switching frequency and modulation rate 1/512 of switching frequency to reduce the conducted EMI.

The SCT2464 offers cycle-by-cycle current limit and hiccup over current protection, thermal shutdown protection, output over-voltage protection and input voltage under-voltage protection. The device is available in 3.5mm*4mm QFN-14L package.

Typical Application Circuit



3.5V-36V, Syncronous Buck Converter



Efficiency, V_{OUT}=5V, Fsw=400KHz

RT/SYNC	6	Set the internal oscillator clock frequency or synchronize to an external clock. Connect a resistor from this pin to ground to set switching frequency. An external clock can be input directly to this pin. The internal oscillator synchronizes to the external clock frequency with PLL. If detected clocking edges stops, the operation mode automatically returns to resistor adjusted frequency.
EN	7	Enable pin to the regulator with internal pull-up current source. Pull below 1.1V to disable the converter. Float or connect to VIN to enable the converter. The tap of resistor divider from VIN to GND connecting EN pin can adjust the input voltage lockout threshold.
VIN1	8	Input supply to the converter. Connect a high-quality bypass capacitor or capacitors from this pin to PGND1. Low impedance connection must be provided to VIN2.
PGND1	9	Power ground to internal low-side MOSFET. Connect to system ground. Low impedance connection must be provided to PGND2. Connect a high-quality bypass capacitor or capacitors from this pin to VIN1.
SW	10	Regulator switching output. Connect SW to an external power inductor
PGND2	11	Power ground to internal low-side MOSFET. Connect to system ground. Low impedance connection must be provided to PGND1. Connect a high-quality bypass capacitor or capacitors from this pin to VIN2.
VIN2	12	Input supply to the converter. Connect a high-quality bypass capacitor or capacitors from this pin to PGND2. Low impedance connection must be provided to VIN1.
BOOT	13	Power supply bias for high-side power MOSFET gate driver. Connect a 0.1uF capacitor from BOOT pin to SW pin. Bootstrap capacitor is charged when low-side power MOSFET is on or SW voltage is low.
NC	14	Not Connection.

Recommended Operating Conditions

Over operating free-air temperature range unless otherwise noted

PARAMETER	DEFINITION	MIN	MAX	UNIT
V_{IN}	Input voltage range	3.5	36	V
V_{OUT}	Output voltage range	1	36	V
T_J	Operating junction temperature	-40	150	°C

ESD Ratings

PARAMETER	DEFINITION	MIN	MAX	UNIT
V_{ESD}	Human Body Model(HBM)	-2	+2	kV
	Charged Device Model(CDM)	-1	+1	kV

Thermal Information

PARAMETER	THERMAL METRIC	QFN-14L	UNIT
$R_{\theta JA}$	Junction to ambient thermal resistance(1)	48.5	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	2.51	
Ψ_{JB}	Junction-to-board characterization parameter(1)	4.46	
$R_{\theta JC\_top}$	Junction to case thermal resistance(1)	30.98	
$R_{\theta JB}$	Junction-to-board thermal resistance(1)	4.55	

(1) SCT provides $R_{\theta JA}$ and $R_{\theta JB}$ numbers only as reference to estimate junction temperatures of the devices. $R_{\theta JA}$ and $R_{\theta JB}$ are not a characteristic of package itself, but of many other system level characteristics such as the design and layout of the printed circuit board (PCB) on which the SCT2464 is mounted, thermal pad size, and external environmental factors. The PCB board is a heat sink that is soldered to the leads and thermal pad of the SCT2464. Changing the design or configuration of the PCB board changes the efficiency of the heat sink and therefore the actual $R_{\theta JA}$ and $R_{\theta JB}$.

Electrical Characteristics

V_{IN}=24V, T_A=-40°C~125°C, typical value is tested under 25°C.

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
Power Supply						
V_{IN}	Operating input voltage		3.5		36	V
I_{SHDN}	Shutdown current from VIN pin	EN=0		1.8		A
I_{Q_BIAS}	Quiescent current from VIN pin	EN floating, non-switching, VBIAS=5V, BOOT-SW=5V		13		A
I_Q	Quiescent current from VIN pin	EN floating, non-switching, BOOT-SW=5V		45	120	

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
V_{PG_OV}	Power-good flag over voltage tripping threshold	POWER BAD (% of FB voltage)		110		%
		POWER GOOD (% of FB voltage)		105		%
I_{PG}	PWRGD leakage current at high level output	VPull-Up = 5V			200	nA
V_{PG_LOW}	PWRGD low level output voltage	IPull-Up = 1 mA		0.05		V
$t_{PGDFLT(rise}$	Delay time to PGOOD high signal			2		ms
$t_{PGDFLT(fall}$	Glitch filter time constant for PGOOD function			100		us
Protection						
V_{OVP}	Feedback overvoltage with respect to reference voltage	V_{FB}/V_{REF} rising		110		%
		V_{FB}/V_{REF} falling		105		%
V_{BOOTUV}	BOOT-SW UVLO Threshold	BOOT-SW falling		2.35		V
		Hysteresis		250		mV
T_{SD}	Thermal shutdown threshold*	T_J rising		172		°C
		Hysteresis		12		°C

C

SIFDOCFKDUDF HULV LFVC

Figure 2. Efficiency, F_{SW}=400KHz, V_{OUT}=5V(BIAS)

Figure 3. Efficiency, F_{SW}=400KHz, V_{OUT}=5V(NO BIAS)

Figure 4. Efficiency, F_{SW}=400KHz, V_{OUT}=3.3V

Figure 5. Efficiency, F_{SW}=1.8MHz, Vin=12V

Figure 6. Load Regulation (Vout=5V)

Figure 7.Clock Frequency vs RT/CLK Resistor

C C

I X F IR DOCEORFNGGID UDP C

C

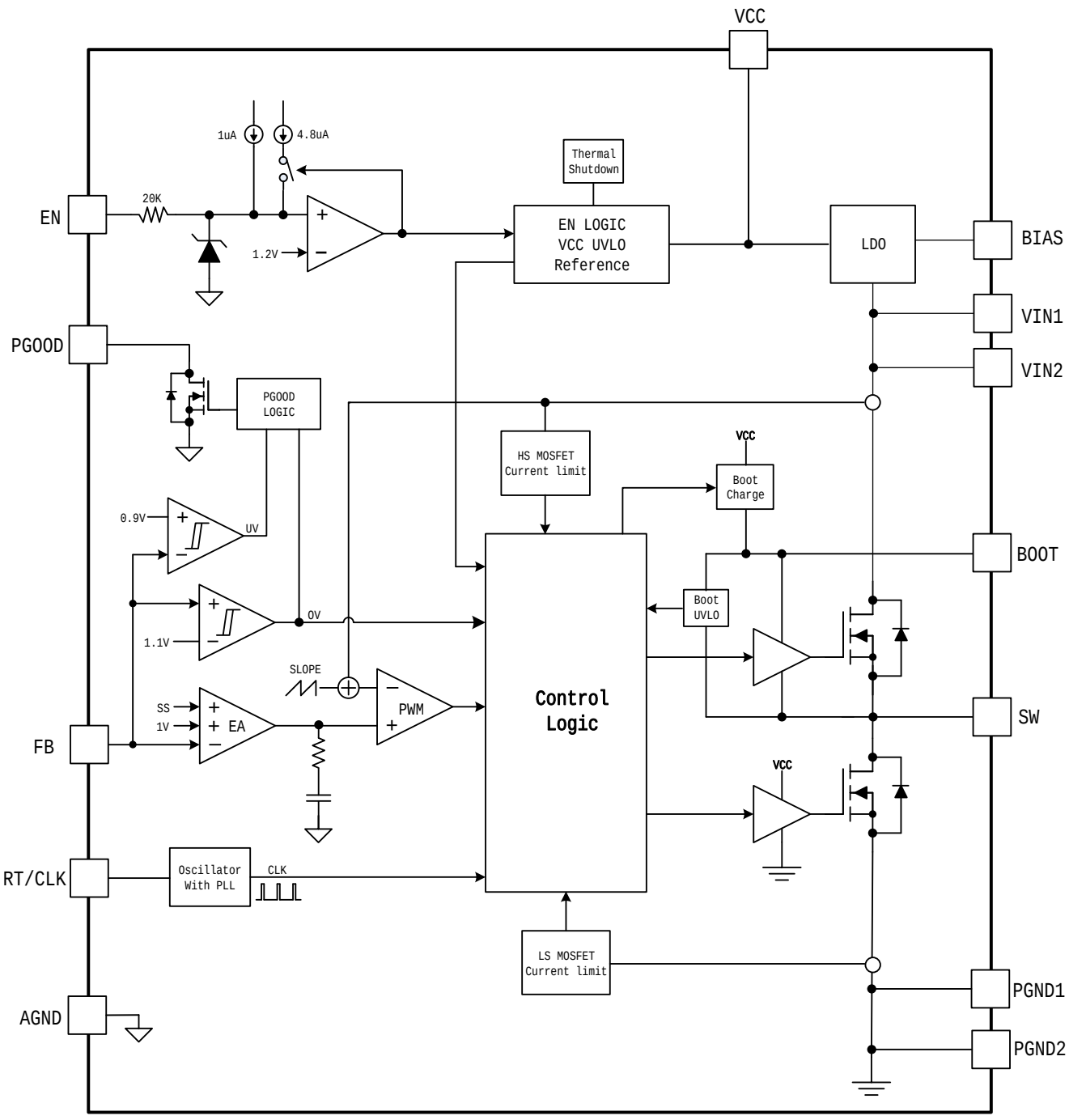


Figure 8. Functional Block Diagram

RSHUD IR C

Overview

The SCT2464 is a 3.5V-36V input, 6A output, EMI friendly synchronous buck converter with built-in 30m Rdson high-side and 18m Rdson low-side power MOSFETs. It implements constant frequency peak current mode control to regulate output voltage, providing excellent line and load transient response and simplifying the external frequency compensation design.

The switching frequency is adjustable from 200kHz to 1.8MHz with two setting modes, resistor setting frequency mode and the clock synchronization mode, to optimizes either the power efficiency or the external component sizes. The SCT2464 features an internal 2ms soft-start time to avoid large inrush current and output voltage overshoot during startup. The device also supports monolithic startup with pre-biased output condition. The seamless mode-transition between PWM mode and PSM mode operations ensure high efficiency over wide load current range. The quiescent current is typically 13uA (VBIAS=5V) under no load or sleep mode condition to achieve high efficiency at light load.

The EN pin is a high-voltage pin with a precision threshold that can be used to adjust the input voltage lockout thresholds with two external resistors to meet accurate higher UVLO system requirements. Floating EN pin enables the device with the internal pull-up current to the pin. Connecting EN pin to VIN directly starts up the device automatically.

The SCT2464 implements the Frequency Spread Spectrum FSS modulation spreading of ±6% centered selected switching frequency. FSS improves EMI performance by not allowing emitted energy to stay in any one receiver band for a significant length of time.

The SCT2464 full protection features include the input under-voltage lockout, the output over-voltage protection, over current protection with cycle-by-cycle current limiting and hiccup mode, output hard short protection and thermal shutdown protection.

Peak Current Mode Control

The SCT2464 employs fixed frequency peak current mode control. An internal clock initiates turning on the integrated high-side power MOSFET Q1 in each cycle, then inductor current rises linearly. When the current through high-side MOSFET reaches the threshold level set by the COMP voltage of the internal error amplifier, the high-side MOSFET turns off. The synchronous low-side MOSFET Q2 turns on to the next clock cycle begins or the inductor current falls to zero.

The error amplifier serves the COMP node by comparing the voltage of the FB pin with an internal 1.0

Enable and Under Voltage Lockout Threshold

The SCT2464 is enabled when the VCC pin voltage rises above 3.3V and the EN pin voltage exceeds the enable threshold of 1.25V. The device is disabled when the VCC pin voltage falls below 3.1V or when the EN pin voltage is below 1.05V. An internal 250A pull up current source to EN pin allows the device enable when EN pin floats.

EN pin is a high voltage pin that can be connected to VIN directly to start up the device.

For a higher system UVLO threshold, connect an external resistor divider (R1 and R2) shown in Figure 9 from VIN to EN. The UVLO rising and falling threshold can be calculated by Equation 1 and Equation 2 respectively.

— (1)

— (2)

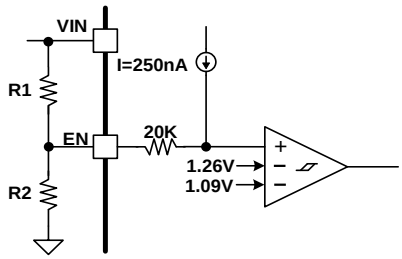


Figure 9. System UVLO by enable divide

where

V_{rise} is rising threshold of Vin UVLO

V_{fall} is falling threshold of Vin UVLO

V_{ENR}=1.25V, V_{ENF}=1.05V

Output Voltage

The SCT2464 regulates the internal reference voltage at 1.0V with 1.5% tolerance over the operating temperature and voltage range. The output voltage is set by a resistor divider from the output node to the FB pin. It is recommended to use 1% tolerance or better resistors. Use Equation 3 to calculate resistance of resistor dividers. To improve efficiency at light loads, larger value resistors are recommended. However, if the values are too high, the regulator will be more susceptible to noise affecting output voltage accuracy.

—— (3)

where

R_{FB_TOP} is the resistor connecting the output to the FB pin.

R_{FB_BOT} is the resistor connecting the FB pin to the ground.

Internal Soft-Start

The SCT2464 integrates an internal soft-start circuit that ramps the reference voltage from zero volts to 1.0V reference voltage in 4mS. If the EN pin is pulled below 1.12V, switching stops and the internal soft-start resets. The soft-start also resets during shutdown due to thermal overloading.

Switching Frequency and Clock Synchronization

The switching frequency of the SCT2464 is set by placing a resistor between RT/CLK pin and the ground, or synchronizing to an external clock.

In resistor setting frequency mode, a resistor placed between RT/SYNC pin to the ground sets the switching frequency over a wide range from 200KHz to 1.8MHz. The RT/SYNC pin voltage is typical 0.5V. RT/SYNC pin is not allowed to be left floating or shorted to the ground. Use Equation 4 or the plot in Figure 10. to determine the resistance for a switching frequency needed.

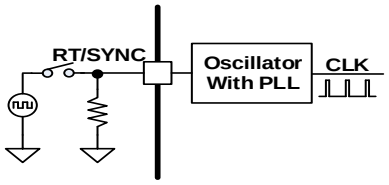


Figure 10. Setting Frequency and Clock Synchronization

where, fsw is switching clock frequency

In clock synchronization mode, the switching frequency synchronizes to an external clock applied to RT/SYNC pin. The synchronization frequency range is from 200KHz to 1.8MHz and the rising edge of the SW synchronizes to the falling edge of the external clock at RT/SYNC pin with typical 66ns time delay. A square wave clock signal to RT/SYNC pin must have high level no lower than 3V, low level no higher than 0.4V, and pulse width larger than 100ns (TYP).

In applications where both resistor setting frequency mode and clock synchronization mode are needed, the device can be configured as shown in Figure 10. Before an external clock is present, the device works in resistor setting frequency mode. When an external clock presents, the device automatically transitions from resistor setting mode to external clock synchronization mode. An internal phase locked loop PLL locks internal clock frequency onto the external clock within typical 85us. The converter transitions from the clock synchronization mode to the resistor setting frequency mode when the external clock disappears.

Frequency Spread Spectrum

To reduce EMI, the SCT2464 implements Frequency Spread Spectrum (FSS). The FSS circuitry shifts the switching frequency of the regulator periodically within a certain frequency range around the adjusted switching frequency. The jittering span is ±6% of the switching frequency with 1/512 swing frequency. This frequency dithering function is effective for both frequency adjusted by resistor placed at RT/CLK pin and an external clock synchronization application.

VCC LDO, VCC UVLO, and BIAS Input

The VCC pin is the output of the internal LDO used to supply the control circuits of the SCT2464 and the typical output voltage is 4.2V. The BIAS pin is the input of the internal LDO. This input can be connected to V_{OUT} to save the power loss from V_{IN}. If the BIAS voltage is larger than 4.8V, LDO is powered by BIAS pin. If the BIAS voltage is less than 4.6 V, VIN1 and VIN2 directly powers the internal LDO. To prevent unsafe operation, VCC has a UVLO that prevents switching if the internal voltage is too low.

Bootstrap Voltage Regulator and Low Drop-out Operation

An external bootstrap capacitor between BOOTock

during slowing power-up and power-down application, the off-time of the high side MOSFET starts to approach the minimum value. Without LDO operation mode, beyond this point the switching may become erratic and/or the

Once the FB pin is between 95% and 105% of the internal voltage reference the PGOOD pin is de-asserted and the pin floats with 2ms delay. The PGOOD pin is pulled low when the FB is lower than 90% or greater than 110% of the nominal internal reference voltage with 100us deglitching time,PG_OVP only work in the close-loop state . Also, the PWRGD is pulled low if VIN UVLO or thermal shutdown are asserted or the EN pin pulled low, Output voltage excursions that are shorter than 100us deglitching time do not trip the PGOOD flag.

Thermal Shutdown

The SCT2464 protects the device from the damage during excessive heat and power dissipation conditions. Once the junction temperature exceeds 172°C, the internal thermal sensor stops power MOSFETs switching. When the junction temperature falls below 160°C, the device restarts with internal soft start phase.

DSSOLFD IR CL IRUP D IR C

Typical Application

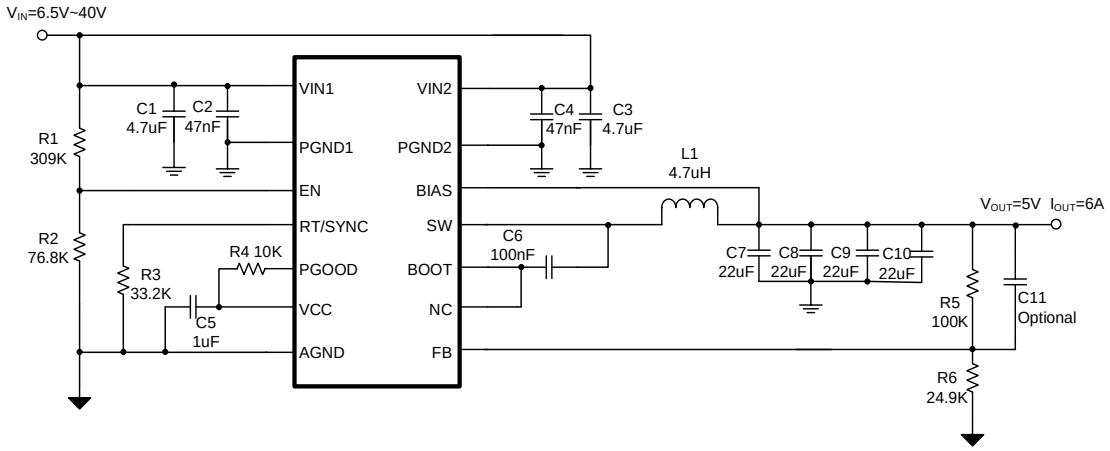


Figure 12. SCT2464 Design Example, 5V Output with Adjustable UVLO

Design Parameters

Design Parameters	Example Value
Input Voltage	24V Normal 3.5V to 36V
Output Voltage	5V
Maximum Output Current	6A
Switching Frequency	400 KHz
Output voltage ripple (peak to peak)	6.2mV
Transient Response 1.5A to 4.5A load step	Vout = 300mV
Start Input Voltage (rising VIN)	6.3V
Stop Input Voltage (falling VIN)	5.5V

Output Voltage

The output voltage is set by an external resistor divider R5 and R6 in typical application schematic. Recommended R6 resistance is 24.9K . Use equation 5 to calculate R5.

V_{ENR}=1.25V, V_{ENF}=1.05V

Inductor Selection

There are several factors should be considered in selecting inductor such as inductance, saturation current, the RMS current and DC resistance(DCR). Larger inductance results in less inductor current ripple and therefore leads to lower output voltage ripple. However, the larger value inductor always corresponds to a bigger physical size, higher series resistance, and lower saturation current. A good rule for determining the inductance to use is to allow the inductor peak-to-peak ripple current to be approximately 20%~40% of the maximum output current.

The peak-to-peak ripple current in the inductor I_{LPP} can be calculated as in Equation 9.

(9)

Where

I_{LPP} is the inductor peak-to-peak current
L is the inductance of inductor
f_{SW} is the switching frequency
V_{OUT} is the output voltage
V_{IN} is the input voltage

Since the inductor-current ripple increases with the input voltage, so the maximum input voltage in application is always used to calculate the minimum inductance required. Use Equation 10 to calculate the inductance value.

(10)

Where

L_{MIN} is the minimum inductance required
f_{sw} is the switching frequency
V_{OUT} is the output voltage
$V_{IN(max)}$ is the maximum input voltage
$I_{OUT(max)}$ is the maximum DC load current
LIR is coefficient of I_{LPP} to I_{OUT}

The total current flowing through the inductor is the inductor ripple current plus the output current. When selecting an inductor, choose its rated current especially the saturation current larger than its peak operation current and RMS current also not be exceeded. Therefore, the peak switching current of inductor, I_{LPEAK} and I_{LRMS} can be calculated as in equation 11 and equation 12.

(11)

(12)

Where

I_{LPEAK} is the inductor peak current
I_{OUT} is the DC load current
I_{LPP} is the inductor peak-to-peak current
I_{LRMS} is the inductor RMS current

In overloading or load transient conditions, the inductor peak current can increase up to the switch current limit of the device which is typically 8A. The most conservative approach is to choose an inductor with a satu

(16)

Where

is the output voltage ripple
f_{SW} is the switching frequency
L is the inductance of inductor
C_{OUT} is the output capacitance
V_{OUT} is the output voltage
$V_{IN}$is the input voltage

Due to degrading under DC bias, the bias voltage can significantly reduce capacitance. Ceramic capacitors can lose most of their capacitance at rated voltage. Therefore, leave margin on the voltage rating to ensure adequate effective capacitance. Typically, two 47

Table 3: Typical External Component Values

	57.6					
	57.6					
	274					
	274					

Application Waveforms

Vin=24V, Vout=5V, unless otherwise noted

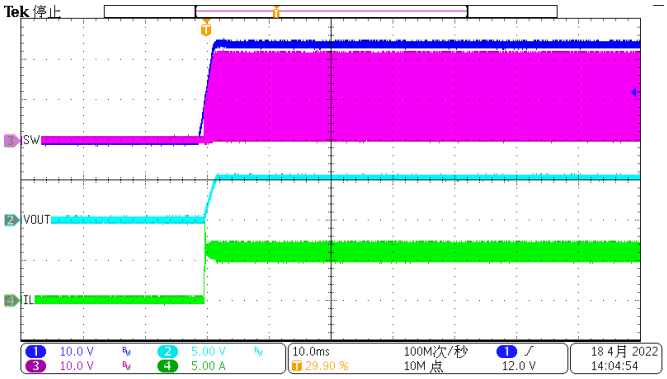


Figure 13. Power up(Iload=6A)

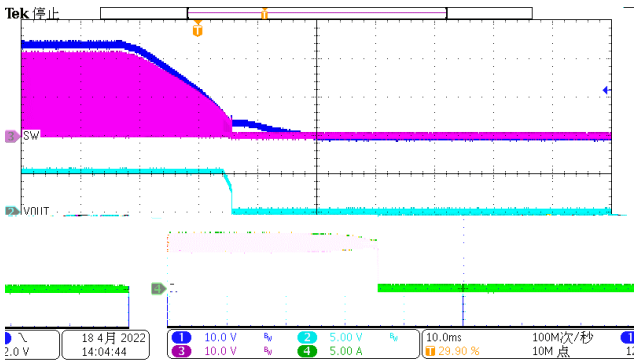


Figure 14. Power down(Iload=6A)

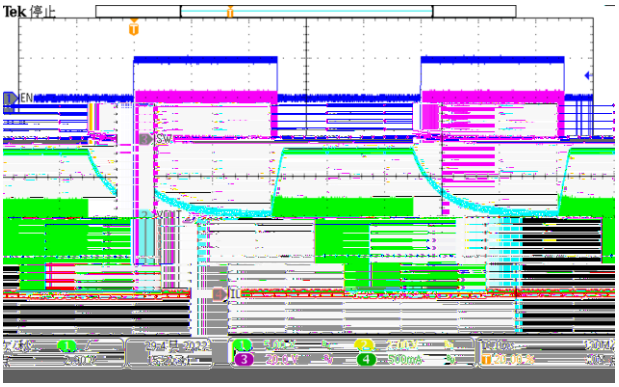


Figure 15. EN toggle (Iload=0.1A)

Figure 16. EN toggle (Iload=6A)

Figure 17. Over Current Protection(1A to hard short)

Figure 18. Over Current Release (hard short to 1A)

Application Waveforms

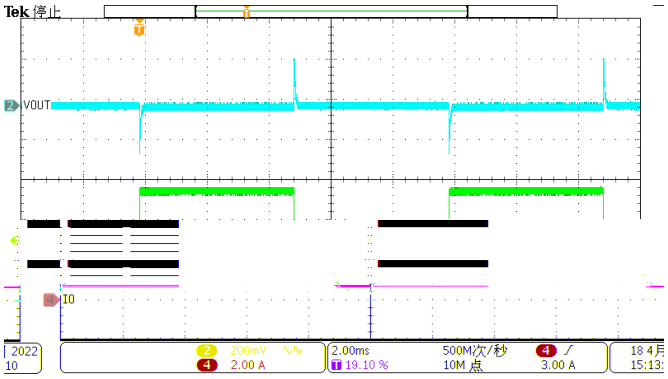


Figure 19. Load Transient (0.6A-5.4A, 1.6A/us)

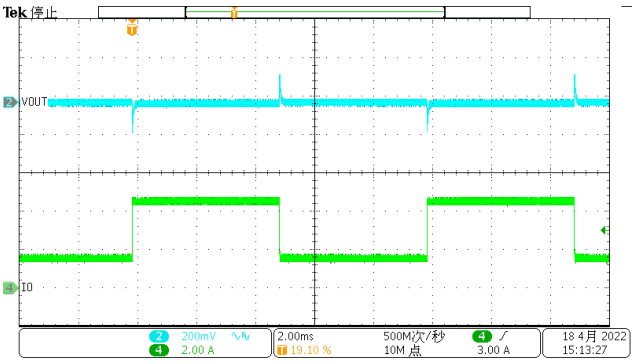


Figure 20. Load Transient (1.5A-4.5A, 1.6A/us)

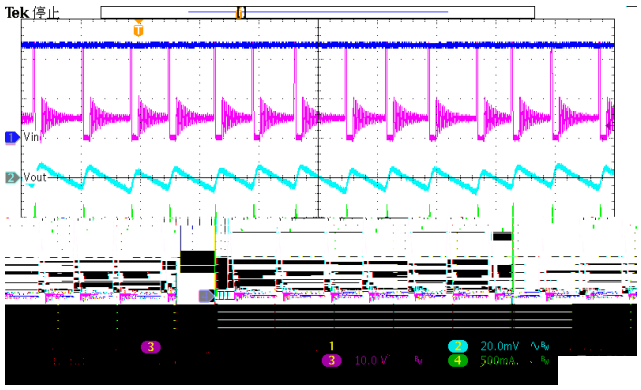


Figure 21. Output Ripple (Iload=100mA)

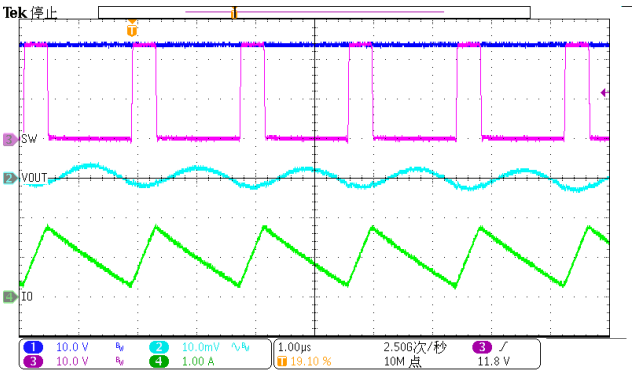


Figure 22. Output Ripple (Iload=1A)

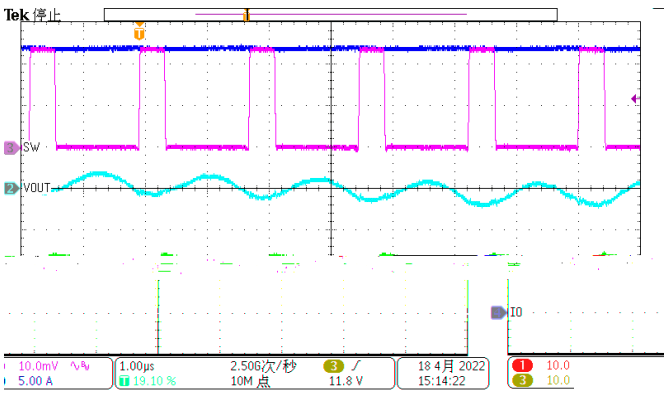


Figure 23. Output Ripple (Iload=6A)

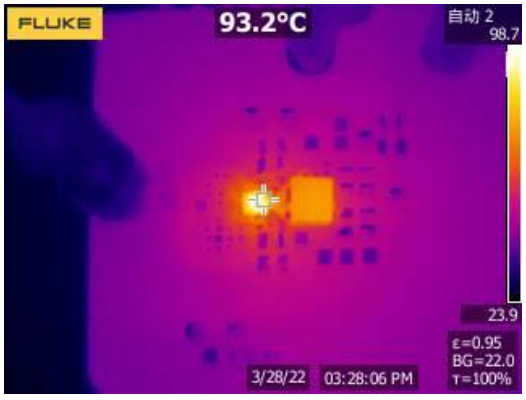


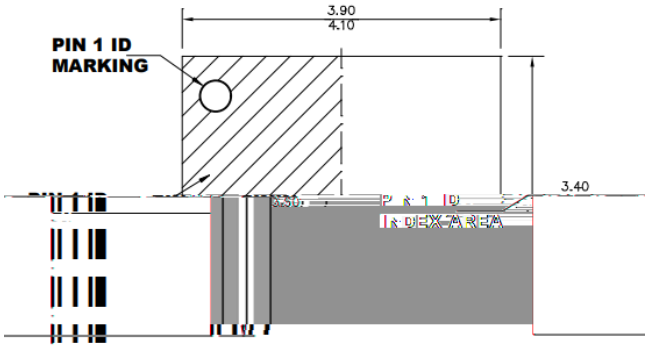
Figure 24. Thermal,12Vin,5Vout,6A

Layout Guideline

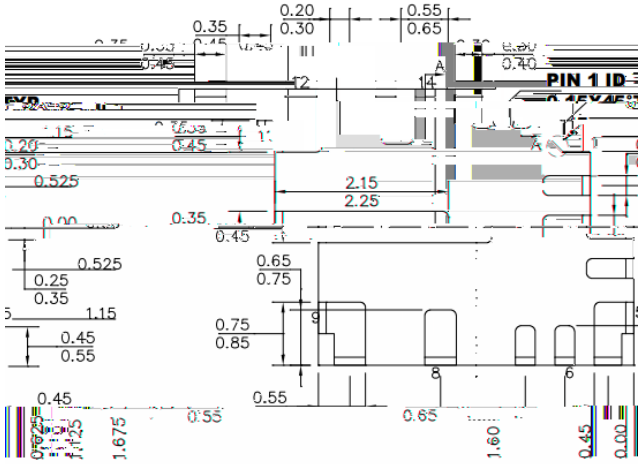
Proper PCB layout is a critical for SCT2464 . The traces conducting fast switching currents or voltages are easy to interact with stray inductance and parasitic capacitance to generate noise and degrade performance. For better results, follow these guidelines as below:

1. Power grounding scheme is very critical because of carrying power, thermal, and glitch/bouncing noise associated with clock frequency. The thumb of rule is to make ground trace lowest impendence and power are distributed evenly on PCB. Sufficiently placing ground area will optimize thermal and not causing over heat area.
2. Place a low ESR ceramic capacitor as close to VIN pin and PGND as possible to reduce parasitic effect.
3. Output inductor should be placed close to the SW pin. The area of the PCB conductor minimized to prevent excessive capacitive coupling.
4. The RT/SYNC

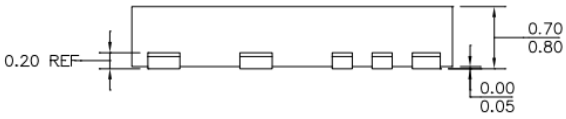
SDFND HCL IRUP D IR



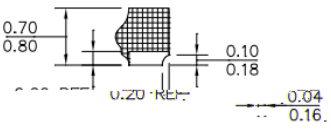
TOP VIEW



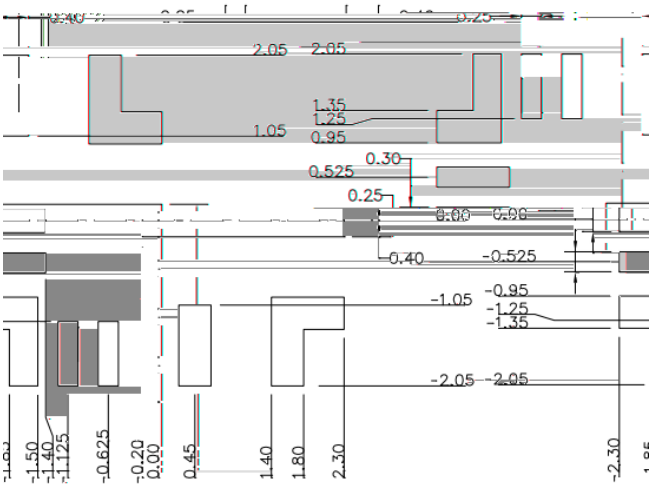
BOTTOM VIEW



SIDE VIEW



SECTION A-A



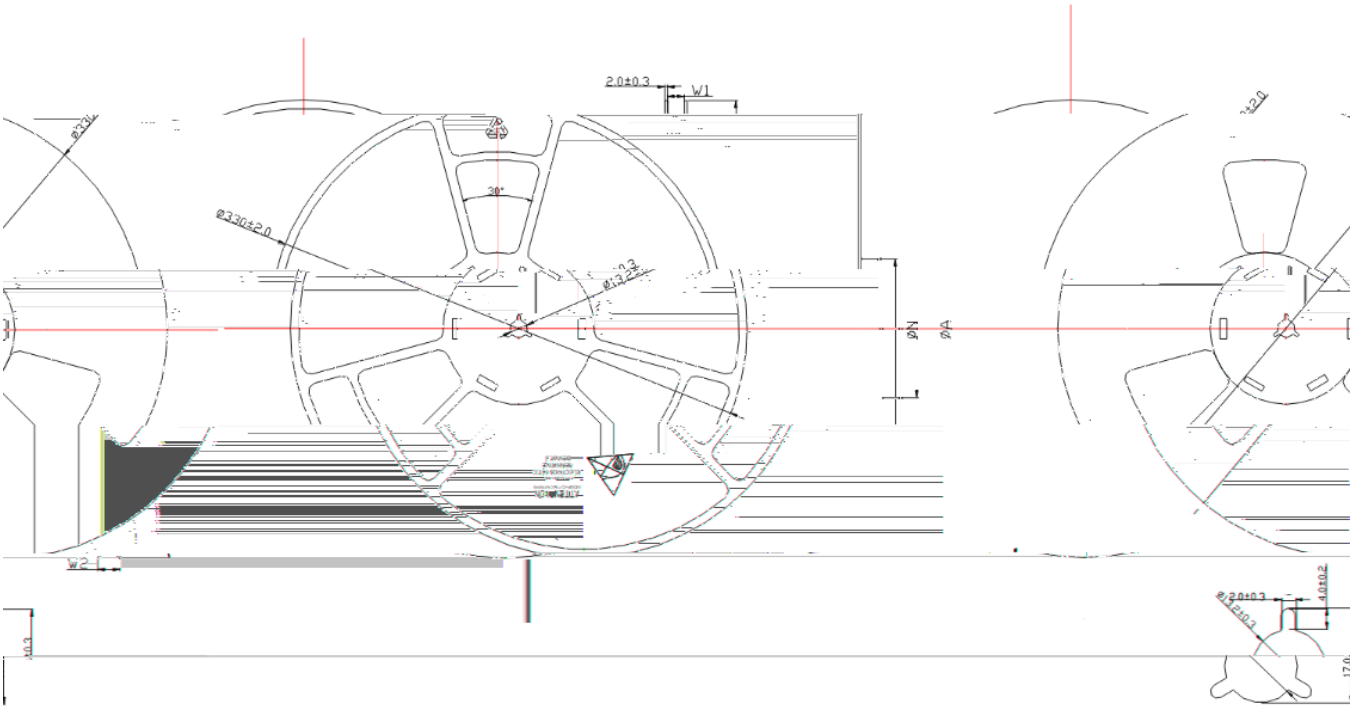
RECOMMENDED LAND PATTERN

QFN-14L (3.5*4) Package Outline Dimensions

NOTE:

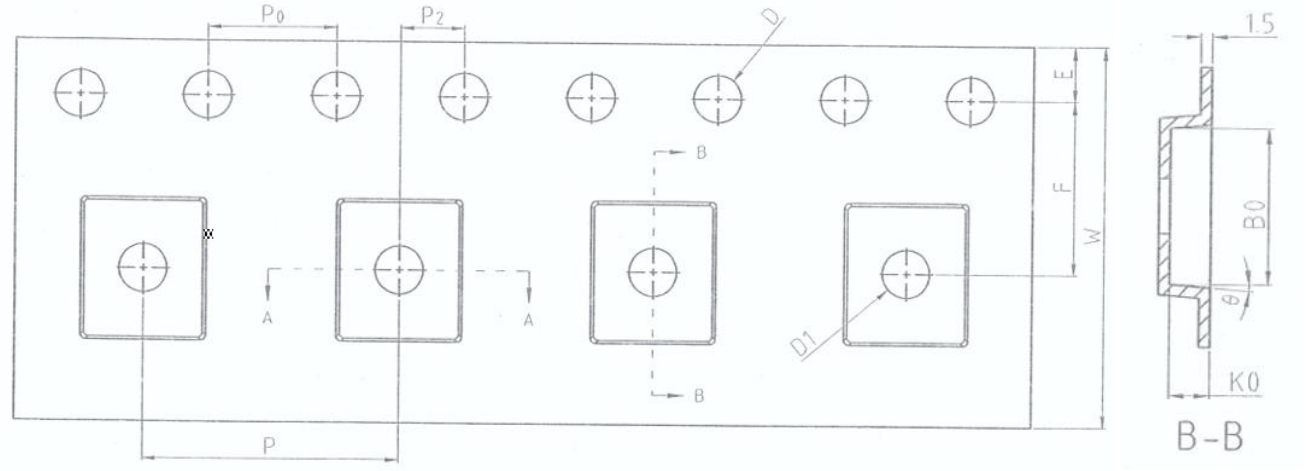
1. THE LEAD SIDE IS WETTABLE.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
4. JEDEC REFERENCE IS MO-220.
5. DRAWING IS NOT TO SCALE.

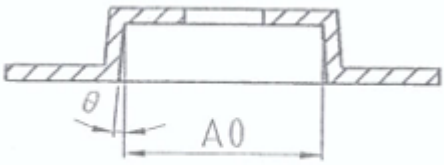
DSHD GCUHHOL IRUP D LR C



PRODUCT SPECIFICATIONS				
TYPE WIDTH	ØA	Ø N	W1(Min)	W2(Max)
12MM	330±2.0	100±1.0	12.4	19.4
[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
[illegible]	24MM	330±2.0	100±1.0	24.4	[illegible]
[illegible]	32MM	330±2.0	100±1.0	32.4	[illegible]
100±1.0	44.4	51.4	44MM	330±[illegible]

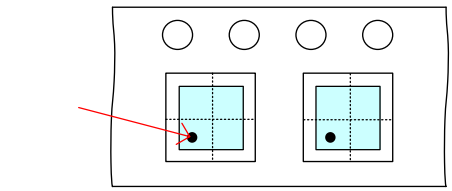
DSHD GCUHHOL IRUP D IR C





A-A

Feeding Direction



外观	尺寸 (MM)
E	1.75±0.10
F	5.50±0.05
P2	2.00±0.05
D	1.55±0.05

外观	尺寸 (MM)
W	$12.00^{+0.30}_{-0.10}$
P	8.00±0.10
A0	3.75±0.10
B0	4.25

