36V Vin Quad Channels PMIC for Safety Applications

FEATURES

Qualified for Automotive Applications
AEC-Q100 Qualified with the Following Results:
- Device Temperature Grade 1

Wide Input Voltage Range: 3.5V-36V

One Synchronous HV Buck Converter VOUT1:
- Up to 3A Continuous Output Current
- Output Voltage of 3.3V

Dual Synchronous LV Buck Converters VOUT2, VOUT3:
- Up to 2A Continuous Output Current
- Output Voltage Range 0.8V to 2.35V with 50mV Steps

One Synchronous LV Boost converter VOUT4:
- Up to 500mA Continuous Output Current
- Output Voltage of 5V

+/- 1.5% Feedback Reference Voltage

Fixed 2.2MHz Switching Frequency with Integrated Frequency Dither for EMI Mitigation

FCCM/PFM Selectable

Programmable Power Sequencer for VOUT2, VOUT3 and VOUT4

RESETB Output for System Management

External Voltage Monitor

Sequencer Output

External Clock Synchronization

Simple/QA Watchdog

Integrated Protection Features:
- Hiccup Over Current Protection
- Output Over-voltage/Under-voltage Protection
- Adjustable Input Voltage Under-voltage Lockout
- Thermal Shutdown Protection

Functional Safety Features:
- Compliance with ISO26262 Development
- Hardware Integrity up to Support ASIL-B System
- ASIL-B Device Certification by TUV
- BIST

Up to 1MHz I2C Interface with Optional Packet Error-Checking (PEC)

Available in FCQFN-24 (4mm*4mm)

DESCRIPTION

The SCT61440S device is a wide input power management IC with four channels output. The device is designed for SoCs in automotive and industrial radar applications.

The SCT61440S integrates one 3A HV Buck, two identical 2A LV Buck and a 500mA LV Boost. Each channel output is continuously monitored, any over-voltage/under-voltage fault will be detected and the device will enter RESET state. All output voltages are pre-programmed, which saves external feedback divider and minimizes system solution. The switching frequency of HV Buck is 2.2MHz/400kHz selectable. The switching frequency is fixed 2.2MHz for LV buck and boost converters. The device features Frequency Spread Spectrum (FSS) with programmable jittering span of the switching frequency and modulation frequency to reduce the conducted EMI.

The device also integrates simple watchdog mode and QA watchdog mode. The dedicated WDI pin allows trigger pulse generated by MCU. Programmable watchdog window is suitable for a wide variety of applications. The RESETB output can be the sequencer of MCU to protect it from device fault.

The SCT61440S device has protection features such as thermal shutdown, short-circuit protection and over-voltage protection. Disabling all outputs via I2C can reduce the quiescent current to 0.85 mA.

The device has Built-in Self-Test (BIST) Diagnosis over internal analog and digital circuits. All critical comparator and data will be checked during power up stage.

The device is available in a FCQFN-24(4mm*4mm) Package.

APPLICATIONS

ADAS
77GHz Radar
Safety MCU

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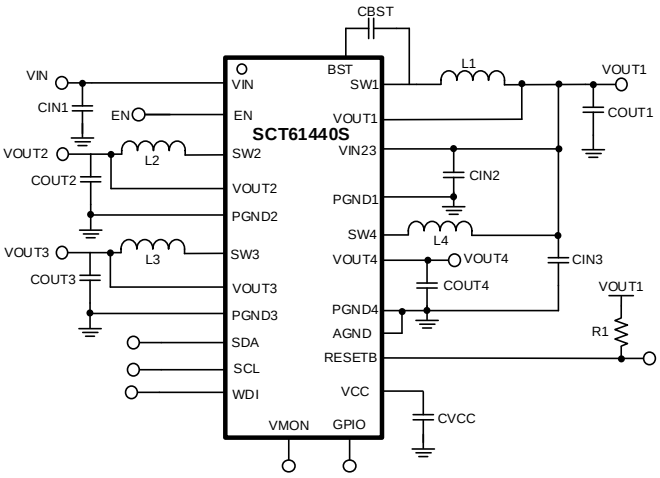
TYPICAL APPLICATION



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REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version

Revision 1.0: Released to Market

Revision 1.1: Add VMON lkg in EC, update thermal resistance, correct typo

Revision 1.2: Update SCT61440S-0059 VOUT2 to 1.15V, correct package marking, correct package description add SS time limit in EC

DEVICE ORDER INFORMATION

PART NUMBER	PACKAGINCE OAGIOet (N)-66.2602 NUMBER

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RECOMMENDED OPERATING CONDITIONS

Over operating free-air temperature range unless otherwise noted

PARAMETER	DEFINITION	MIN	MAX	UNIT
V_{IN}	Input voltage range	3.5	36	V
V_{OUT2}	LV Buck2 Output voltage range	0.8	2.35	V
V_{OUT3}	LV Buck3 Output voltage range	0.8	2.35	V
T_J	Operating junction temperature	-40	150	°C

ESD RATINGS

PARAMETER	DEFINITION	MIN	MAX	UNIT
V_{ESD}	Human Body Model(HBM), per AEC-Q100-002	-2	+2	kV
	Charged Device Model(CDM), per AEC-Q100-011	-1	+1	kV

THERMAL INFORMATION

PARAMETER	THERMAL METRIC	FCQFN-24	UNIT
R - $	Junction to ambient thermal resistance(1)	39.68	°C/W
JT	Junction-to-top characterization parameter	1.78	
JB	Junction-to-board characterization parameter(1)	3.26	
R - &(top)	Junction to case (top) thermal resistance(1)	24.67	
R -B	Junction to board thermal res[illegible]	[illegible]	

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ELECTRICAL CHARACTERISTICS

V_{IN}=12V, T_J=-40°C~150°C, typical values are tested under 25°C.

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
Power Supply and Output						
V_{IN}	Operating input voltage		3.5		36	V
$V_{IN\_UVLO\_RISING}$	Input UVLO rising threshold	VIN_START[1:0]=00b	3	3.2	3.4	V
		VIN_START[1:0]=01b	3.8	4	4.2	V
		VIN_START[1:0]=10b	4.8	5	5.2	V
		VIN_START[1:0]=11b	5.8	6	6.2	V
$V_{IN\_UVLO\_FALLING}$	Input UVLO falling threshold	VIN_STOP[1:0]=00b	2.5	2.8	3.1	V
		VIN_STOP[1:0]=01b	3.2	3.5	3.8	V
		VIN_STOP[1:0]=10b	4.2	4.5	4.8	V
		VIN_STOP[1:0]=11b	5.2	5.5	5.8	V
V_{IN_OVP}	Input OVP	V_{IN} rising	40	43	45	V
$V_{IN\_OVP\_HYS}$	Hysteresis			3		V
I_{SD}	Shutdown current	EN low		0.5	10	A
I_Q	Quiescent current from VIN	No load, FCCM, V_{OUT1} = 3.3V(1)		20		mA
		No load, PFM, V_{OUT1} = 3.3V(1)		1		mA
		All channels off via I2C		0.85	2	mA
VCC Power						
V_{CC}	Internal linear regulator		4.5	4.7	4.9	V
V_{CC_UVLO}	VCC UVLO	V_{CC} rising	2.6	2.8	3	V
$V_{CC\_UVLO\_HYS}$	Hysteresis			200		mV
V_{CCOV_THR}	VCC OV Threshold	V_{CC} rising	5	5.3	5.6	V
V_{CCOV_HYS}	Hysteresis			250		mV
IV_{CC}	VCC sourcing current limit	V_{CC} = 4.4V		70		mA
Enable and RESETB						
V_{EN_H}	Enable high threshold	V_{EN} ramping up		1.2	1.4	V
V_{EN_L}	Enable low threshold	V_{EN} ramping down	0.8	1.0		V
R_{EN_DOWN}	Enable pin pull-down resistance			2.1		M Ÿ
T_{RSTB}	RESETB pin holding time	RESETB_HT[1:0]=00b		10		ms
		RESETB_HT[1:0]=01b		20		
		RESETB_HT[1:0]=10b		30		
		RESETB_HT[1:0]=11b		40		
I_{RST_LKG}	Output-High leakage current				1	uA
V_{RST_L}	RESETB output low level	Sinking -2mA			0.2	V
VOUT1 (HV Buck)						
V_{ACC1}	Voltage accuracy	T_J = 25°C	-1		1	%
		T_J = -40°C~150°C	-1.5		1.5	%

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ELECTRICAL CHARACTERISTICS (continued)

V_{IN}=12V, T_J=-40°C~150°C, typical values are tested under 25°C.

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
R_{DSON_H1}	High-side MOSFET on-resistance	V_{BOOT}-V_{SW}=5V		75	150	m Ÿ
R_{DSON_L1}	Low-side MOSFET on-resistance			50	120	m Ÿ
I_{LIM_HS1}	High-side power MOSFET current limit		4.2	5.2	6.2	A
I_{LIM_LSP1}	Low-side power MOSFET positive current limit		3.2	4.2	5.2	A
I_{LIM_LSN1}	Low-side power MOSFET negative current limit		0.8	2	3.2	A
R_{DIS1}	Discharge resistance	Output disabled		100	200	Ÿ
t_{ON_MIN1}	Minimum on-time			80		ns
$_{Phase1}$(1)	Switching phase			0		deg
VOUT2 (LV Buck)						
V_{S2}(1)	Supply voltage range		3		5.5	V
V_{ACC2}	Voltage accuracy	T_J = 25°C T_J = -40°C~150°C	-1 Ŧ	2	1 T	% T m

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ELECTRICAL CHARACTERI

V_{IN}=12V, T_J=-40°C~150°C, typical

SYMBOL	PARAMETER	TION	MIN	TYP	MAX	UNIT
R_{DIS3}	Discharge resis	d		55	100	Ÿ
t_{ON_MIN3}	Minimum on-tir			90		ns
$_{Phase3}$(1)	Switching phas			180		deg
VOUT4 (LV Boost)						
V_{S4}(1)	Supply voltage		3		4.5	V
V_{ACC4}	Voltage accura		-1		1	%
		°C	-1.5		1.5	%
R_{DSON_H4}	High-side MOS resistance			180	280	m Ÿ
R_{DSON_L4}	Low-side MOS resistance			60	100	m Ÿ
I_{LIM_LS4}	Low-side powe current limit		1.4	2	2.6	A
I_{LIM_HSP4}	High-side powe current limit		0.9	1.4	1.9	A
I_{LIM_HSN4}	High-side powe negative curren		200	500	800	mA
R_{DIS4}	Discharge resis	d		200	300	Ÿ
t_{ON_MIN4}	Minimum on-tir			80		ns
$_{Phase4}$(1)	Switching phas			180		deg
Soft Start and Delay						
T_{SS}	Soft-start time	option 0	0.5	1	1.5	ms
		option 1	0.2	0.5	0.8	ms
T_{EN_ON}(1)	Device on time			2.8		ms
T_{ON_DELAY2}(1)	On delay for V		0		75	ms
T_{ON_DELAY3}(1)	On delay for V		0		75	ms
T_{ON_DELAY4}(1)	On delay for V		0		75	ms
T_{ON_SEQ}(1)	On delay for SI		0		75	ms
Switching Frequency						
F_{SW}	LV Buck&Boos frequency		1.98	2.2	2.42	MHz
F_{SW1}	HV Buck switcl	y option	1.98	2.2	2.42	MHz
		option	360	400	440	kHz
F_{FSS_RERIOD}	Frequency sp period	[0]=0b		4.5		kHz
		[0]=1b		10		
F_{FSS_RANGE}	Frequency spr	>>Bp2 186 >>BDC0.48 re f 135.72 173. 37-0 0 18 16.2				

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ELECTRICAL CHARACTERISTICS (continued)

V_{IN}=12V, T_J=-40°C~150°C, typical values are tested under 25°C.

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
R_{SYNC}	SYNC Input Pulldown	EN high		1.8		M Ÿ
F_{SYNC_RANGE}(1)	SYNC Input Frequency Range	50% duty cycle	1.5		3	MHz
V_{SYN_HI}	Threshold for synchronization	SYNC voltage rising			1.3	V
V_{SYN_LO}		SYNC voltage falling	0.7			V
VMON						
$V_{MONRANGE}$	VMON monitor range		0.6		2.5	V
V_{MONACC}	VMON OV/UV accuracy		-1.5		1.5	%
I_{RST_LKG}	Input leakage current	VMON=1V		4	20	uA

$V_{MONOVTH}$ 0.2 9.548 1.77 6.99 (MO 0 10.8VM)-1.3 (O) <</MCH0 Tc 0 Tw 0.832 0 Td ( )Tj4 (2)Tj -0.1.4 (V)0.5 (a)-2.9 (BDC 8.713 0 T)Tj 0.557 0 TTw 0.532 0 Td 5 0 Tc 27Tw 4.132 o >

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ELECTRICAL CHARACTERISTICS (continued)

V_{IN}=12V, T_J=-40°C~150°C, typical values are tested under 25°C.

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
V_{WDI_LO}		WDI voltage falling	0.8	1		V
$T_{WDI\_DEG\_RISING}$	Deglitch time for WDI pin	WDI voltage rising		30		μs
T_{WD}	Watchdog timer accuracy		-10		10	%
I2C Interface						
V_{IH}	High-level input voltage		1.2			V
V_{IL}	Low-level input voltage				0.4	V
V_{OL}	Low-level output voltage	I_{SINK}=4mA			0.4	V
F_{SCL}(1)	SCL clock frequency				1	MHz
T_{LOW}(1)	Low period of the SCL clock		500			ns
T_{HIGH}(1)	High period of the SCL clock		260			ns
T_{HD_STA}(1)	Hold time (repeated) START condition		260			ns
T_{SU_STA}(1)	Set-up time (repeated) START condition		260			ns
T_{HD_DAT}(1)	Data hold time		0			ns
T_{SU_DAT}(1)	Data set-up time		50			ns
T_R(1)	Rise time of both SCL and SDA signals				120	ns
T_F(1)	Fall time of both SCL and SDA signals				120	ns
T_{SU_STO}(1)	Set-up time for STOP condition		260			ns
C_B(1)	Capacitive load for each bus line				550	pF

(1) Guaranteed by sample and design characterization, not tested in production.

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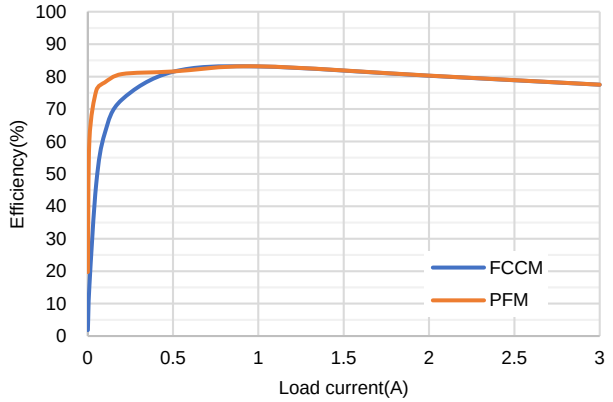
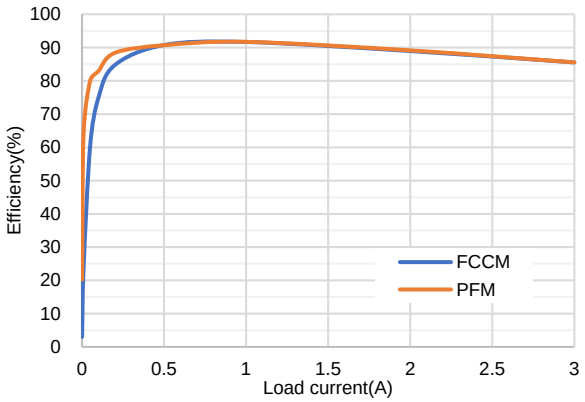
TYPICAL CHARACTERISTICS

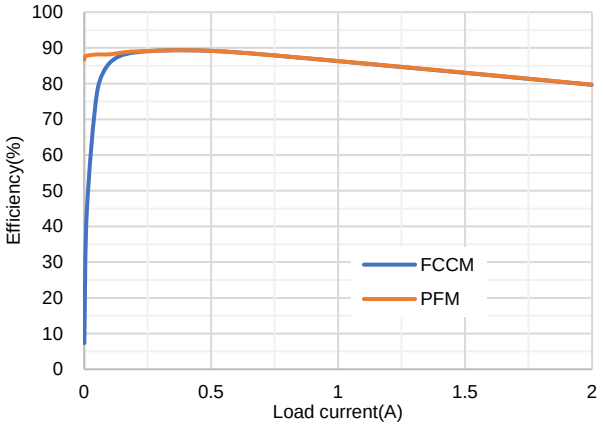
V_{IN}=12V, T_J=-40°C~125°C, unless otherwise noted.



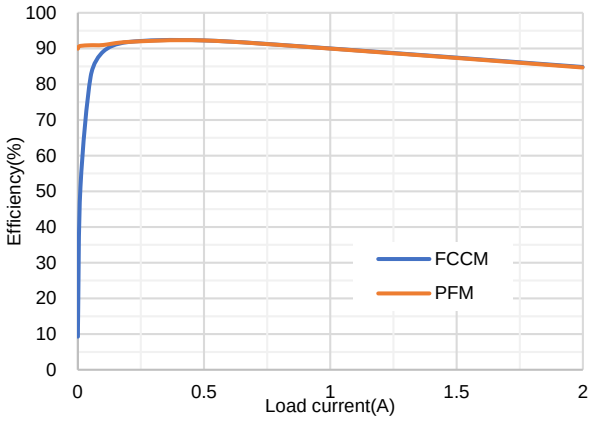
Buck1 Efficiency vs Load Current, V_{OUT1}=3.3V, f_{SW1}=2.2MHz



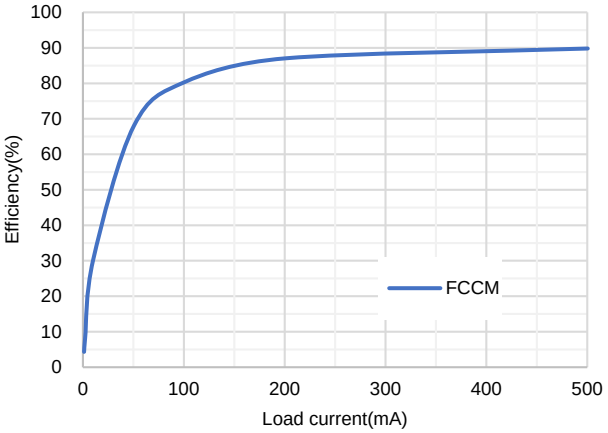
Buck1 Efficiency vs Load Current, V_{OUT1}=3.3V, f_{SW1}=400kHz



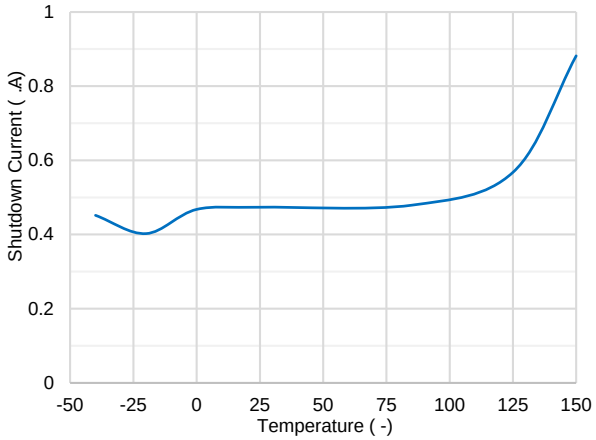
Buck2/3 Efficiency vs Load Current, $V_{OUT2/3}$=1.2V



Buck2 3 Efficiency vs Load Current, $V_{OUT2/3}$=1.8V



Boost Efficiency vs Load Current, V_{OUT4}=5V



Shutdown Current vs Temperature

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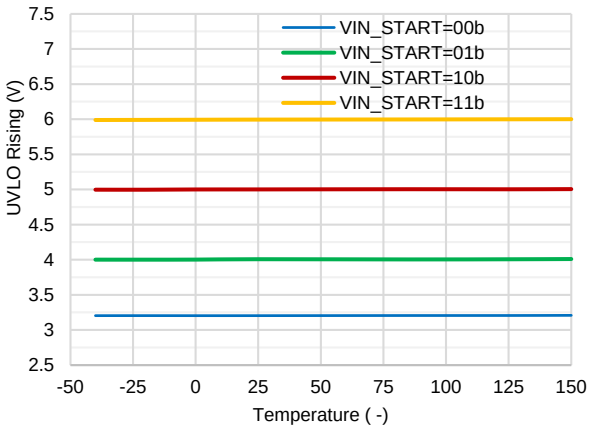
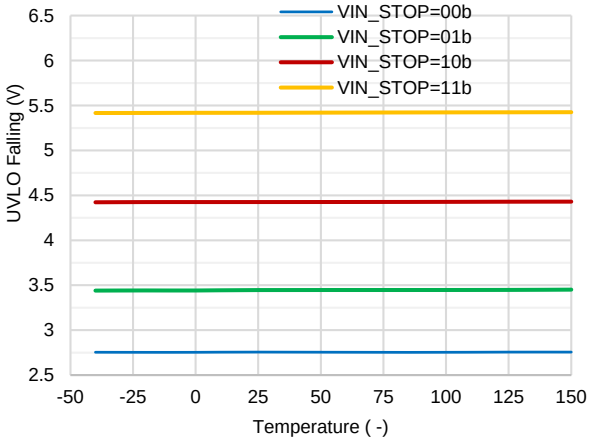
TYPICAL CHARACTERISTICS (continued)

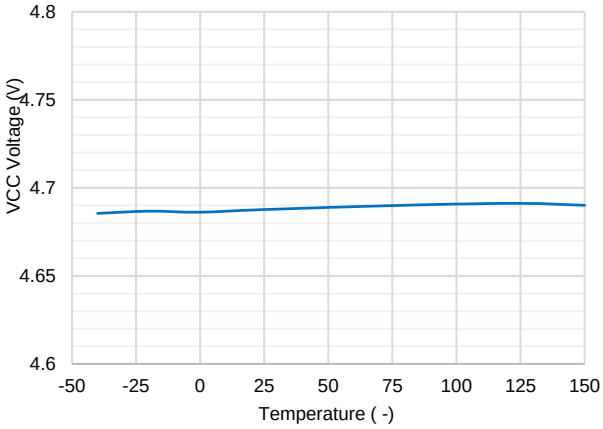
V_{IN}=12V, T_J=-40°C~125°C, unless otherwise noted.



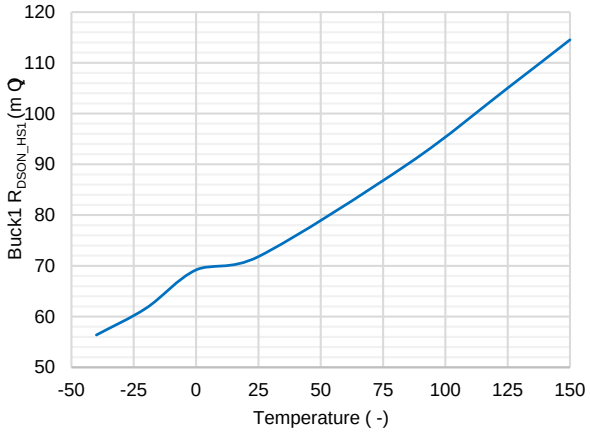
UVLO Rising Threshold vs Temperature



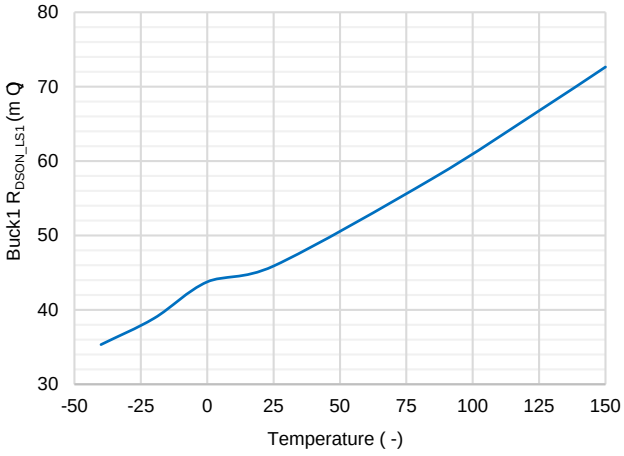
UVLO Falling Threshold vs Temperature



VCC vs Temperature



Buck1 R_{DSON_HS1} vs Temperature



Buck1 R_{DSON_LS1} vs Temperature

Buck2 R_{DSON_HS2} vs Temperature

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FUNCTIONAL BLOCK DIAGRAM

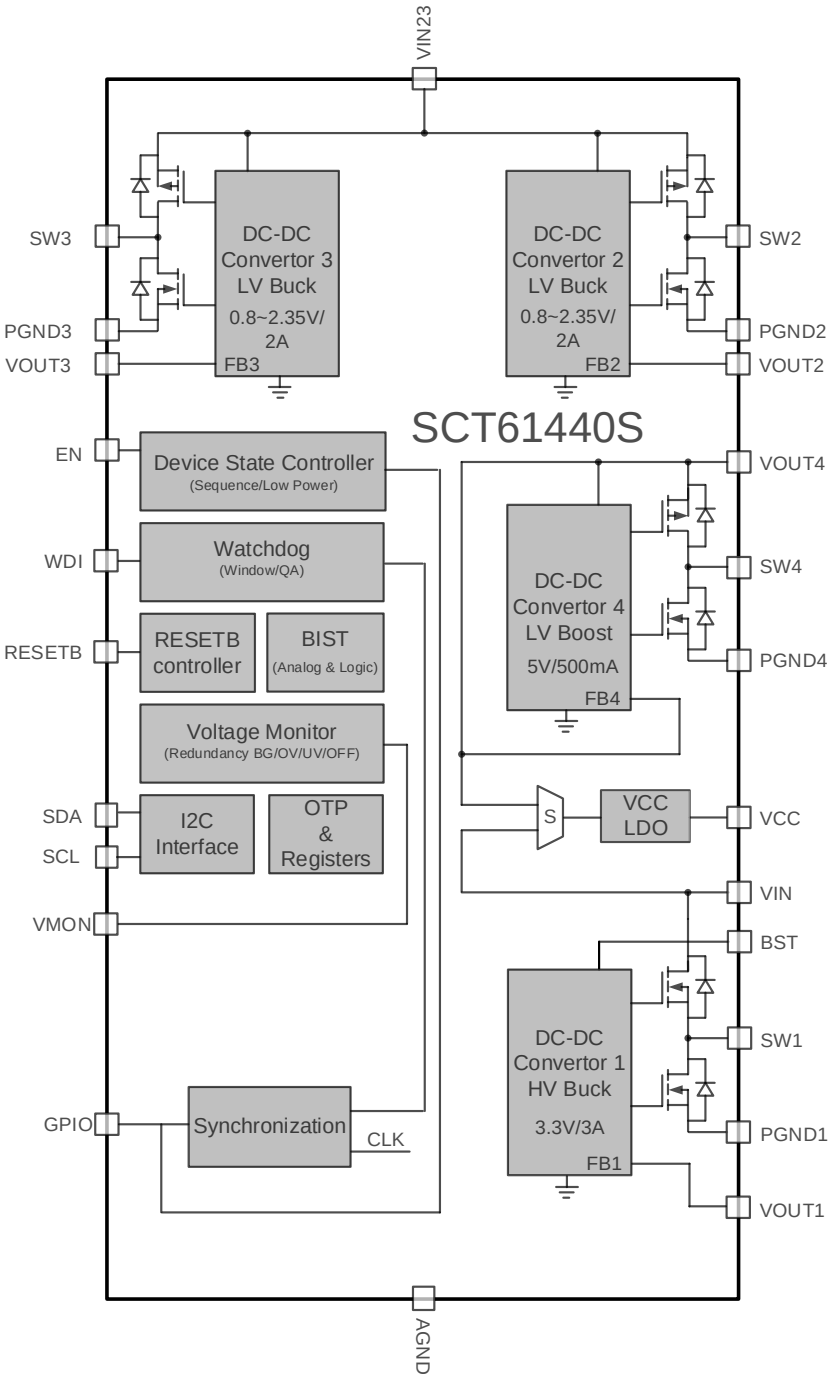

Figure 1. Functional Block Diagram

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OPERATION

Overview

The SCT61440S device is a wide input power management IC with quad channels output. The device is designed for SoCs in automotive and industrial radar applications. The SCT61440S integrates one 3A HV Buck, two identical 2A LV Buck and a 500mA LV Boost. Each channel output is continuously monitored, any over-voltage/under-voltage fault will trigger RESETB pull low. Any deep over-voltage/under-voltage will be detected and the device will enter DEEPSAFE state. All output voltages are pre-programmed, which saves external feedback divider and minimizes system solution. The switching frequency of HV Buck is 2.2MHz/400kHz selectable. The switching frequency is fixed 2.2MHz for LV buck and boost converters. The device features Frequency Spread Spectrum (FSS) with programmable jittering span of the switching frequency and modulation frequency to reduce the conducted EMI.

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The SCT61440S device has protection features such as thermal shutdown, short-circuit protection and over-voltage/under-voltage protection. Disabling all outputs via I2C can reduce the quiescent current to 0.85 mA.

The device has Built-in Self-Test (BIST) Diagnosis over internal analog and digital circuits. All critical comparator and data will be checked before power up stage. Safety features ensure compliance with ISO26262 standard and functional safety up to ASIL-B level.

Operating State Machine

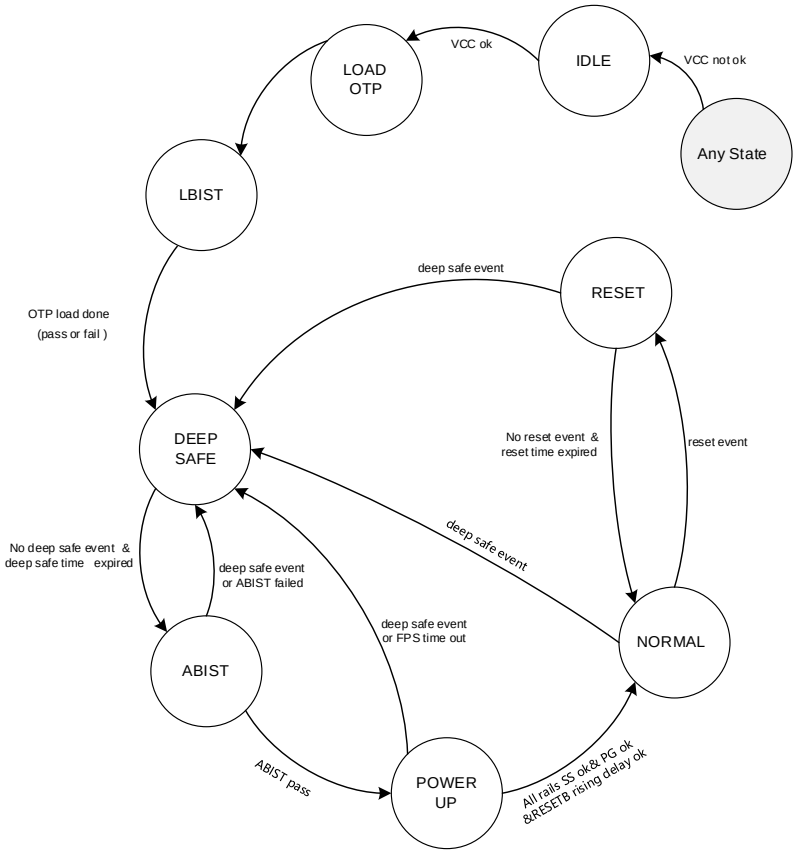

Figure 2. Operating Sate Transitions

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Table 1. Sate and Function Matrix Table

State	Function										
	I2C	OTP load	Register reset	HV BUCK1	LV BUCK2	LV BUCK3	LV BOOST4	Watchdog	OCP	DOVP/DUVP detect	TSD
IDLE	OFF	OFF	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF
LOADOTP	OFF	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF
LBIST	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF
DEEPSAFE	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	ON
ABIST	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	ON
POWERUP	ON	OFF	OFF	UP	UP	UP	UP	OFF	ON	ON	ON
NORMAL	ON	OFF	OFF	ON	ON	ON	ON	ON	ON	ON	ON
RESET	ON	OFF	OFF	ON	ON	ON	ON	OFF	ON	ON	ON

Table 2. Sate and Functional Pin Matrix Table

State	RESETB
IDLE	Tri-state

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VIN/EN UVLO

VCC OVP

VIN OVP

RESETB Stuck

Loss of ground

ABIST State

To ensure safety mechanism work well, the device will check through all critical analog comparators before output start-up. If ABIST check is failed, the device will go back to DEEPSAFE state. ABIST will be implemented every time SCT61440S enter ABIST state, the device will transit to POWERUP state once ABIST is passed. Any ABIST failure will be recorded in register **SYS_STATE**.

POWERUP State

In POWERUP state, all rails will start-up following a dedicated sequence. Since the HV buck VOUT1 is the power supply for the other channels, VOUT1 is always set to start-up first. Then the other channels will rise after turn on delay time respectively. The turn on delay time for each is independent and can be adjusted via changing register **CONFIG_PU1** and **CONFIG_PU2**, thus flexible sequence is available. Deep OV/UV protection is activated to protect channels from destructive OV/UV risk. If all channels finish soft-start and they are within power good range, the RESETB rising timer begins. Once the timer is expired, the device will enter NORMAL state and RESETB will output high. If deep safe event occurs, the state will transit to DEEPSAFE state directly.

NORMAL State

The NORMAL state is the normal running of device with all outputs on. The RESETB pin is released after specific delay time upon entering this state. If watchdog is enabled by register **CONFIG_WD3**, watchdog window will start after setting delay time. The delay time is configured by **WD_1UD[2:0]** in register **CONFIG_WD3**. MCU should feed the watchdog via WDI pin or write answer to specified register periodically. When operating in NOMRAL state, the device will go to RESET state once reset event occurs.

RESET State

All outputs keep on in this state, the device will transit from NORMAL state to RESET state when any of below reset event occurs:

VOUT1’s output is out of OV/UV protection range

VOUT2’s output is out of OV/UV protection range

VOUT3’s output is out of OV/UV protection range

VOUT4’s output is out of OV/UV protection range

VMON voltage is out of OV/UV protection range

Watchdog Failure

When the device enters RESET state, the RESETB pin will assert for a holding time. The device will go back to NORMAL state automatically once the holding time is expired and no reset event, which can be configured in register **CONFIG_T1** via I2C. Upon entering NOMRAL state Watchdog failure counter will be reset and start running again. Then MCU should feed the watchdog again.

VIN and EN UVLO

When the VIN pin voltage rises above 3.2V and the EN pin voltage exceeds the enable threshold of 1.2V, the device is enabled. And the device disables when the VIN pin voltage falls below 2.8V or when the EN pin voltage is below 1.0V.

EN pin is connected internally to ground allows the device to be disabled when EN pin is floating to simplif

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High Efficiency Regulators

The switching frequency of HV Buck is 2.2MHz/400kHz selectable. All the LV bucks and boost employ 2.2MHz fixed frequency peak current mode control. Forced continuous conduction mode (FCCM) allows the device to have a high output performance when light load. Built-in UVLO ensures all channels are capable of regulated output under the operating VIN range. Soft-start is fixed at 1ms for all channels. VOUT1 will always be the firstly built rail after power on, the other rails can be configured with range 0ms to 75ms turn on delay. Then the device can achieve a variety of sequence to fit power system.

The VOUT1 is a HV synchronous buck converter directly power from VIN pin. It's regulated at 3.3V with up to 3A continuous current. An external 100nF ceramic bootstrap capacitor between BST and SW1 pin powers high-side power MOSFET gate driver. The bootstrap capacitor voltage is charged from an integrated voltage regulator when high-side power MOSFET is off and low-side power MOSFET is on. Note VOUT1 is the power supply for VOUT2/3/4.

The VOUT2 and VOUT3 are two identical LV synchronous buck converter power by VOUT1. Their output can be configured via I2C range from 0.8V to 2.35V with 50mV step. Each is capable of 2A continuous current. To further improve the EMI performance, the VOUT2 and VOUT3 will operate with 180 phase-shifted clock.

The VOUT4 is a LV synchronous boost converter also power by VOUT1. It's regulated at 5V with up to 500mA continuous current.

The converters have proprietary designed gate driver scheme to resist switching node ringing without sacrificing MOSFET turn-on and turn-off time, which further erases high frequency radiation EMI noise caused by the MOSFETs hard switching.

Each output voltage is continuously monitored during operation, the OV/UV threshold can be adjusted independently in register **CONFIG_PGSEL1** and **CONFIG_PGSEL2**.

Deep Over Voltage Protection

If any output exceeds the deep over voltage protection threshold 115%, all outputs will shut off for the hiccup time. When hiccup ends, the normal power up sequence will start again following turn on delay setting in register. When entry hiccup, the output discharge will operate during the hiccup time. The threshold can be configured by bits **DEEP_OVP_SEL[1:0]**.

Deep Under Voltage Protection

If an output falls below the deep under voltage protection threshold 75%, all outputs will shut off for the hiccup time. When hiccup ends, the normal power up sequence will start again following turn on delay setting in register. When entry hiccup, the output discharge will operate during the hiccup time. The threshold can be configured by bits **DEEP_UVP_SEL[1:0]**.

Thermal Shutdown

The thermal shutdown protects the device from the damage during excessive heat and power dissipation conditions. Once the junction temperature exceeds 175 , the internal thermal sensor stops power MOSFETs switching. When the junction temperature falls below 155 , the device will restart with internal soft start phase.

Over Current Protection (OCP)

The converters implement over current protection with cycle-by-cycle limiting high-side MOSFET peak current and also low-side MOSFET valley current to avoid inductor current running away during unexpected overload and hiccup protection in output hard short condition. When overload or hard short happens, the converter cannot provide output current to satisfy loading requirement even though the inductor current has already been clamped at over current limitation. Thus, output voltage drops below regulated voltage continuously. When peak current point is kicked for continuous 32 times, the converter stops switching, the device will jump to DEEPSAFE state. The hiccup protection mode greatly reduces the average short circuit current to alleviate thermal issues and protect the regulator.

For the boost, the device provides a load disconnect function, which completely disconnects the output from the input during overload. Then output short to ground fault is protected.

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Frequency Spread Spectrum

To meet CISPR and automotive EMI compliances, the SCT61440S implements Frequency Spread Spectrum (FSS) function. The FSS circuitry shifts the 2.2MHz switching frequency within dedicated range and period triangular or pseudo modulation. Therefore, the SCT61440S can guarantee that the switching frequency does not drop into the 1.8MHz AM band limit.

Frequency Foldback

To avoid meeting minimum on time, the HV buck VOUT1 will reduce switching frequency actively when input voltage rising high. Other channel's frequency is unchanged.

When VIN greatly drops and minimum off time of HV buck VOUT1 is kicked, the VOUT1 enter dropout mode and also reduce its frequency to get max output.

RESETB Indicator

The RESETB indicator will assert when reset event occurs. It will reset MCU if it fails to feed watchdog, MCU then can reloading program to ensure the program run well. The RESETB pin is an open-drain output and can be connected to various I/O level through pull-up resistor. The reset event mapping to RESETB pin can be configured through changing the register **RSTMAP**.

Sequencer Output

When GPIO pin is set to SEQ, the SEQ pin is an open-drain output and can be connected to any 5V or lower rail through an external pull-up resistor. The pin output a high level after preset delay time. The delay time range from 0 to 75ms after VOUT1 is built successfully, see bit **ON_DELAY_SEQ[3:0]** for details.

External Voltage Monitor

The VMON pin can support external device voltage monitoring. When the monitored voltage is out of the VMON OV/UV range, the device enters RESET state. The RESETB will assert to send out warning signal. The OV/UV threshold can be configured via register **CONFIG_PGSEL1**. This function can be controlled through bit **EN_VMON[0]** and online change is not valid. If the VMON is enabled by default, the VMON will begin to monitor after **ON_DELAY_SEQ[3:0]** plus the configured soft-start time 1ms by default(even if the GPIO is not set to SEQ). The reference voltage of VMON range from 0.6V to 2.5V, which is pre-programmed in factory and cannot be changed via register. Note that VMON should be connected to monitored voltage directly. If a resistor divider network is used for higher voltage monitoring, the sink current into VMON pin must be considered and there will be voltage drop.

Active Output Discharge

Once any output is shutoff due to deep safe events or disabled by I2C command, there is an active output discharge path will be turned 3.6 (() (I)3.6volscorlsia regirP <</M 0.0016 -0e of ore 26.1 elly.w rsshA3-1.5 (ct)-1.3 (i)3-17.695 (u)1.3 (I).2 (ct)

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If **WD_MODE[0]** = 1, the device will implement simple watchdog, the MCU should provide trigger pulse to WDI pin or write any byte to specific register **WD_KEY** within the open window. The length of open window and closed window can be configured by I2C. A correct watchdog trigger will restart the whole window cycle immediately. Giving pulse or writing byte to register **WD_KEY** during the closed window will result in **WD_UV[0]** violation and will restart the whole window cycle immediately. If MCU doesn't send high pulse or write byte to **WD_KEY** before the whole window is expired, **WD_EXP[0]** violation occurs. Any violation will make the WD error counter plus one. When WD error counter reaches the **WD_FAIL_CNT[0]** (1 or 2 times), a WD Failure is reported and device enters RESET state.

QA Watchdog

If **WD_MODE[0]** = 0, the device will implement Question and Answer (QA) watchdog and signals on WDI pin are ignored. In QA watchdog mode, MCU should read register **WD_KEY** to get the answer through I2C. Then MCU response the watchdog in open window through writing the specific answer to register **WD_KEY**. A correct watchdog trigger will refresh the whole window cycle immediately and the **WD_KEY** register being updated. Writing the incorrect answer to the **WD_KEY** will result in the value written being ignored and a **WD_LFSR[0]** violation. Writing the correct response during a closed window will result in the write being ignored and a **WD_UV[0]** violation. If MCU doesn't write byte to **WD_KEY** and the whole window is expired, **WD_EXP[0]** violation occurs. LFSR polynomial: x8 + x6 + x5 + x4 + 1. Any violation except **WD_LFSR[0]** violation will make the WD error counter plus one. When WD error counter reaches the **WD_FAIL_CNT[0]** (1 or 2 times), a WD Failure is reported and device enters RESET state.

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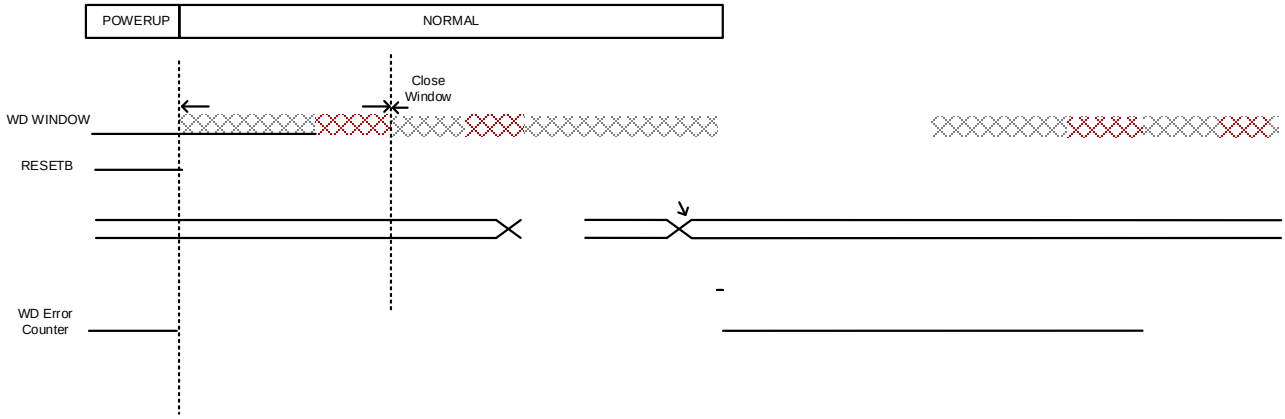

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I2C Interface

The SCT61440S integrates a two-wire serial interface for bidirectional communications between the device and the master through bus. The I2C protocol defines two bus lines, the serial data line (SDA) and the serial clock line (SCL). The SCT61440S is always assigned a unique chip address 0x38 and operates as a slaver, the master drives the SCL line and transfer bidirectional data through SDA line. Both the SCL and SDA lines need a pull-up resistor connected to bus voltage since HIGH state is the default state when bus is idle. The SCT61440S supports Standard-mode (up to 100 kHz), Fast-mode (up to 400 kHz), Fast-mode Plus (up to 1 MHz). The internal filtering ignores spikes and noises on the bus line to preserve data integrity. The maximum capacitive load for each bus line is given in Electrical Characteristic thus the number of interfaces is limited.

Data Validity

The data on the SDA line must be stable during the HIGH period of the clock. The HIGH or LOW state of the data line can only change when the clock signal on the SCL line is LOW.

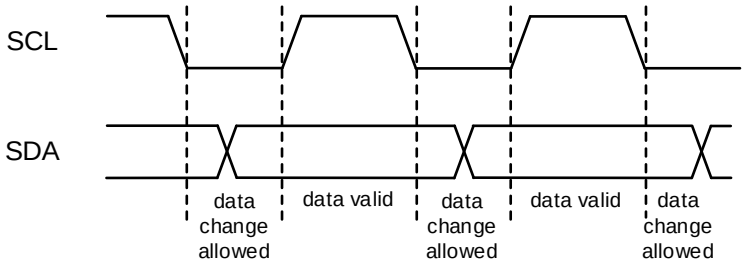

Figure 4. Data Validity Diagram

START and STOP Conditions

The data transfer always generates START and STOP conditions to announce the process. A HIGH to LOW transition on the SDA line while SCL is HIGH defines a START condition. A LOW to HIGH transition on the SDA line while SCL is HIGH defines a STOP condition. Both the START and STOP conditions are generated by master on bus.

The bus is considered to be busy after START condition and released after STOP condition. A repeated START condition during transmission is also valid and will be regard as a new START condition.

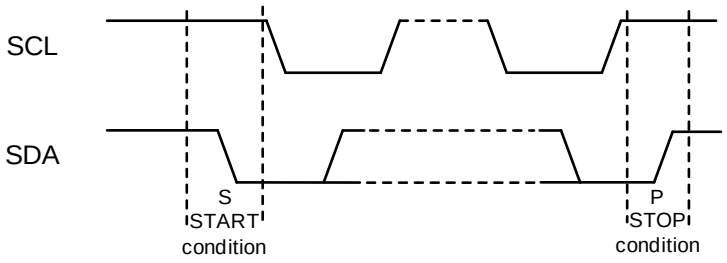

Figure 5. START and STOP Conditions Diagram

Data Transmission

The transferred byte consists of eight bits with the Most Significant Bit (MSB) first. After each byte is transferred, the master will release the SDA line and generate the ninth acknowledge clock pulse on SCL line. The SCT61440S will pull the SDA line LOW during this acknowledge clock, to announce a successful reception and next byte may be sent. If the master is receiver and the last byte is received, it still generates the ninth acknowledge clock pulse but SDA line will not be pulled LOW. It's called not acknowledge signal and indicates the end of transmission.

After the START condition, the master must send a slave address as the first addressing byte. The slave address is seven bits long followed by an eighth R/W bit. The R/W bit defines the data direction. Set the R/W bit to 0 to indicate write command, and a 1 indicates read command. The slave address is factory-programmed between 0x38 through 0x3B, see DEVICE ORDER INFORMATION for details.

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Packet Error Checking (PEC)

The SCT61440S supports optional packet error checking (PEC) byte during the I2C communication. PEC can significantly increase fault coverage on the I2C interface. The PEC byte is implemented through CRC-8 polynomial of x8 + x2 + x +1. The PEC byte does not take ACK, NACK, START, STOP, Repeated START bits into calculation. The PEC byte is calculated on the register address and data byte over the entire message from the first START condition, note that the slave address is removed both in write and read command. When PEC is enabled, the device will reject the write command if the master send an incorrect PEC byte. When in read mode with PEC enabled, the master should acknowledge the data byte thus then the device will send the PEC byte. The PEC can be configured by **PEC_EN** in register **CONFIG_FSS**.

Write Data Format

A write to the device includes transmission of the following:

- START condition
- Slave address with the write bit set to 0
- 1 byte of data to register address
- 1 byte of data to the command register
- STOP condition

Read Data Format

A read from the device includes the following:

- Transmission of a START condition
- Slave address with the write bit set to 0
- 1 byte of data to register address
- Restart condition
- Slave address with read bit set to 1
- 1 byte of data to the command register
- STOP condition

Figure 6 illustrates the proper format for one frame.

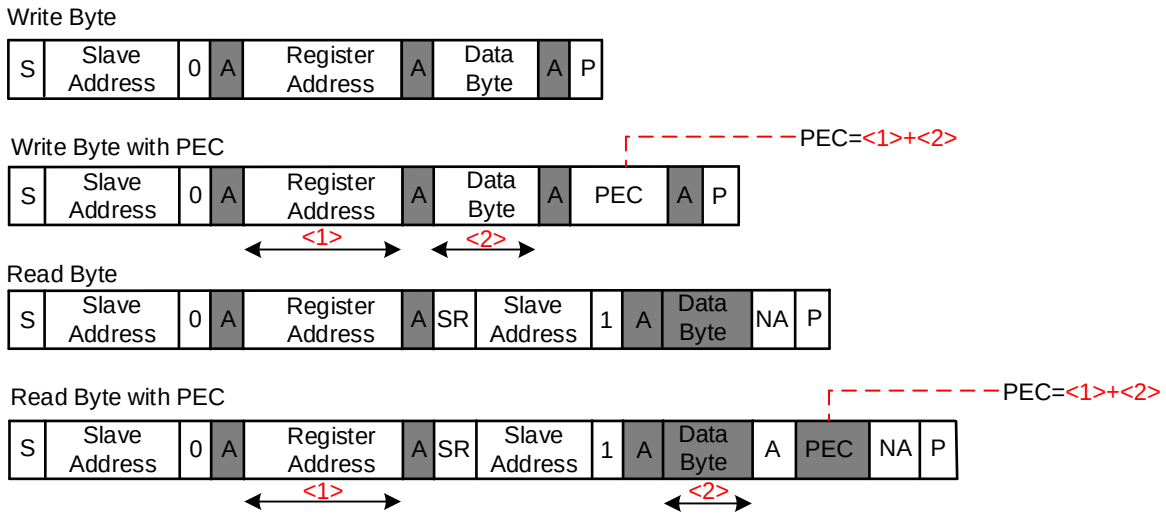

Figure 6. Transmission Data Format Diagram

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APPLICATION INFORMATION

Typical Application

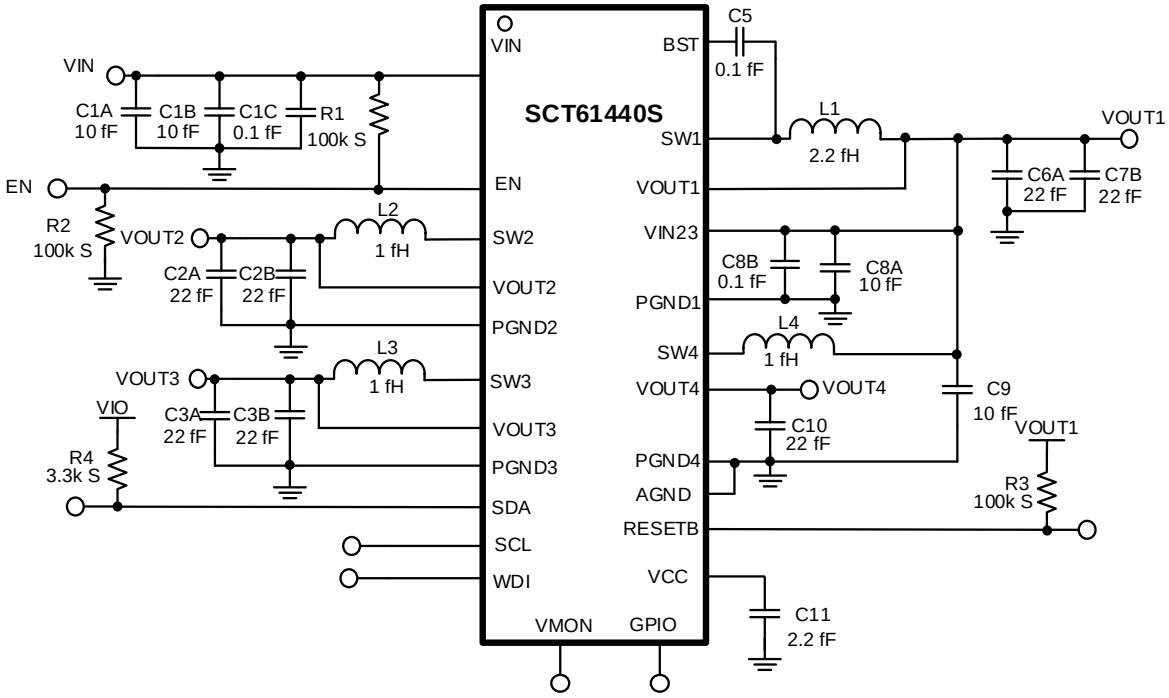

Figure 8. Application Schematic, 3.5V to 36V, PMIC Regulator at 2.2MHz

Design Parameters

Design Parameters	Example Value
Input Voltage	12V Normal 3.5V to 36V
Output Voltage	VOUT1: 3.3V VOUT2: 1.1V VOUT3: 1.5V VOUT4: 5V
Maximum Output Current	VOUT1: 3A (in total) VOUT2: 2A VOUT3: 2A VOUT4: 500mA
Switching Frequency	2.2MHz
Output Voltage Ripple (peak to peak)	VOUT1: 10mV VOUT2: 5mV VOUT3: 5mV VOUT4: 20mV

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Under Voltage Lock-Out

An external voltage divider network of R_1 from the input to EN pin and R_2 from EN pin to the ground can set a higher input voltage's Under Voltage Lock-Out (UVLO) threshold. The UVLO has two thresholds, one for power up when the input voltage is rising and the other for power down or brown outs when the input voltage is falling. Use Equation 1 and Equation 2 to calculate the values of R_1 and R_2 resistors.

$$R_1 = \left(\frac{V_{rise}}{V_{ENrise}} - 1\right) \times R_2 \quad (1)$$

$$R_1 = \left(\frac{V_{fall}}{V_{ENfall}} - 1\right) \times R_2 \quad (2)$$

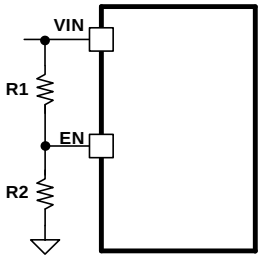

Figure 9. System UVLO by enable divide

where

V_{rise} is rising threshold of Vin UVLO

V_{fall} is falling threshold of Vin UVLO

V_{ENrise} is rising threshold of EN UVLO

V_{ENfall} is falling threshold of EN UVLO

Inductor Selection

There are several factors should be considered in selecting inductor such as inductance, saturation current, the RMS current and DC resistance(DCR). Larger inductance results in less inductor current ripple and therefore leads to lower output voltage ripple. However, the larger value inductor always corresponds to a bigger physical size, higher series resistance, and lower saturation current. A good rule for determining the inductance to use is to allow the inductor peak-to-peak ripple current to be approximately 20%~40% of the maximum output current.

For a buck converter, the peak-to-peak ripple current in the inductor I_{LPP} can be calculated as in Equation 3.

$$I_{LPP\_BUCK} = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{f_{SW} \times V_{IN} \times L} \quad (3)$$

Where

I_{LPP_BUCK} is the inductor peak-to-peak current of buck

L is the inductance of inductor

f_{SW} is the switching frequency

V_{OUT} is the output voltage

V_{IN} is the input voltage

Since the inductor-current ripple increases with the input voltage, so the maximum input voltage in application is always used to calculate the minimum inductance required. Use Equation 4 to calculate the inductance value.

$$L_{MIN} = \frac{V_{IN(max)}}{f_{SW} \times 4 \times I_{OUT(max)}} \times \left(1 - \frac{V_{IN(max)}}{V_{OUT}}\right) \quad (4)$$

Where

L_{MIN} is the minimum inductance required

$V_{IN(max)}$ is the maximum input voltage

$I_{OUT(max)}$ is the maximum DC load current

LIR is coefficient of I_{LPP} to I_{OUT}

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The total current flowing through the inductor is the inductor ripple current plus the output current. When selecting an inductor, choose its rated current especially the saturation current larger than its peak operation current and RMS current also not be exceeded. Therefore, the peak switching current of inductor, I_{LPEAK} and I_{LRMS} can be calculated as in equation 5 and equation 6.

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$$I_{CIN} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}})} \quad (10)$$

The worst case condition occurs at $V_{IN}=2*V_{OUT}$, where:

$$I_{CIN} = 0.5 \times I_{OUT} \quad (11)$$

For simplification, choose an input capacitor with an RMS current rating greater than half of the maximum load current.

When selecting ceramic capacitors, it needs to consider the effective value of a capacitor decreasing as the DC bias voltage across a capacitor increasing.

The input capacitance value determines the input ripple voltage of the regulator. The input voltage ripple can be calculated using Equation 12 and the maximum input voltage ripple occurs at 50% duty cycle.

$$\Delta V_{IN} = \frac{I_{OUT}}{F_{SW} \times C_{IN}} \times \frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (12)$$

For the boost converter power stage, because of the inductor current ripple, the input voltage changes if there is parasitic inductance and resistance between the power supply and the inductor. It is recommended to have enough input capacitance to make the input voltage ripple less than 100mV. Generally, a 10) input capacitance is recommended for most applications. Choose the right capacitor value carefully by considering high-capacitance ceramic capacitors DC bias effect, which has a strong influence on the final effective capacitance.

Bootstrap Capacitor Selection

$) F H U D P L F F D S D F L W R U P X V W S E H F R Q Q H F W H G E H W Z H H Q W K H % 2 2 W S L Q D Q G 6 Z S L Q W R S U R Y L G H D V W D E O H 9 ' ' 2 X W S X W . F H U D P L F capacitor with X5R or better grade dielectric is recommended. The capacitor should have a 10V or higher voltage rating.

Output Capacitor Selection

The selection of output capacitor will affect output voltage ripple in steady state and load transient performance.

For buck converter, the output ripple is essentially composed of two parts. One is caused by the inductor current ripple going through the Equivalent Series Resistance ESR of the output capacitors and the other is caused by the inductor current ripple charging and discharging the output capacitors. To achieve small output voltage ripple, choose a low-ESR output capacitor like ceramic capacitor. For ceramic capacitors, the capacitance dominates the output ripple. For simplification, the output voltage ripple can be estimated by Equation 13 desired.

$$\Delta V_{OUT\_BUCK} = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{8 \times L \times F_{SW}^2 \times C_{OUT} \times V_{IN}} \quad (13)$$

Where

ΔV_{OUT_BUCK} is the output voltage ripple of buck converter

f_{SW} is the switching frequency

L is the inductance of inductor

C_{OUT} is the output capacitance

V_{OUT} is the output voltage

V_{IN} is the input voltage

Due to capacitor's degrading under DC bias, the bias voltage can significantly reduce capacitance. Ceramic capacitors can lose most of their capacitance at rated voltage. Therefore, leave margin on the voltage rating to ensure adequate effective capacitance. Typically, two 10) F H U D P L F R X W S X W F D S D F L W R U V Z R U N

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For boost converter, typically, a 10) F ceramic output capacitors work for most applications. Higher capacitor values can be used to improve the load transient response. From the required output voltage ripple, use the below equation to calculate the minimum required effective capacitance

$$\Delta V_{OUT\_BOOST} = \frac{(V_{OUT} - V_{IN\_MIN}) \times I_{OUT}}{V_{OUT} \times f_{SW} \times C_{OUT}} \quad (14)$$

where

ΔV_{OUT_BOOST} is output voltage ripple caused by charging and discharging of the output capacitor of boost
V_{IN_MIN} is the minimum input voltage of boost converter.
V_{OUT} is the output voltage.
I_{OUT} is the output current.
f_{SW} is the converter switching frequency.

Table 3. Recommended BOM for Typical Application

Output Rail	Frequency (MHz)	L (uH)	Input Capacitor (uF)	Output Capacitor (uF)
Buck1	2.2	2.2	2 x 10+1 x 0.1	2 x 22
Buck2	2.2	1	10+1 x 0.1	2 x 22
Buck3	2.2	1		2 x 22
Boost4	2.2	1	10	22
VCC	-	-	-	2.2

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Application Waveforms

Vin=12V, V_{OUT1}=3.3V, V_{OUT2}=1.1V, V_{OUT3}=1.5V, V_{OUT4}=5V, unless otherwise noted

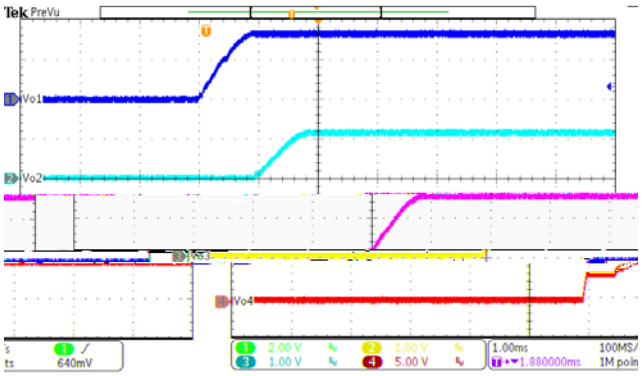

Figure 10. Power On (Io2=Io3=2A, Io4=0.5A)

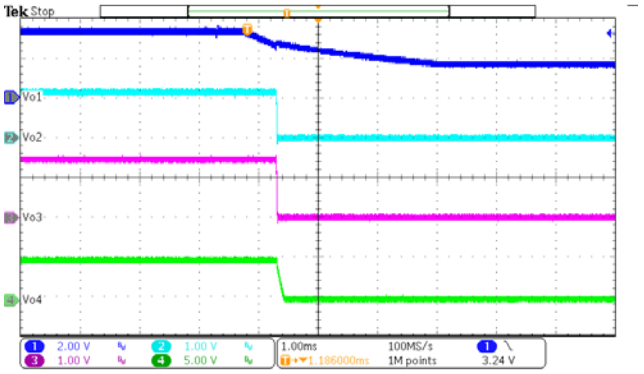

Figure 11. Power Off (Io2=Io3=2A, Io4=0.5A)

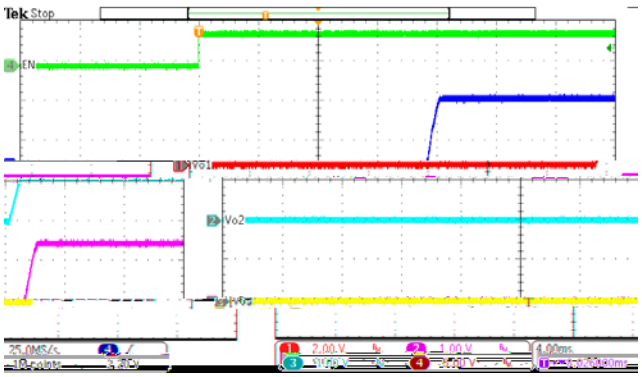

Figure 12. EN On (Io2=Io3=2A, Io4=0.5A)

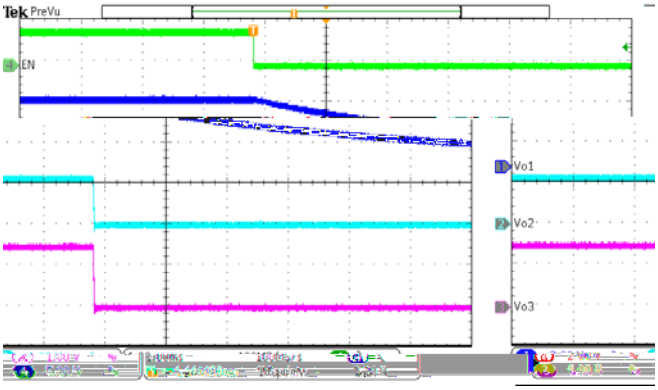

Figure 13. EN Off (Io2=Io3=2A, Io4=0.5A)

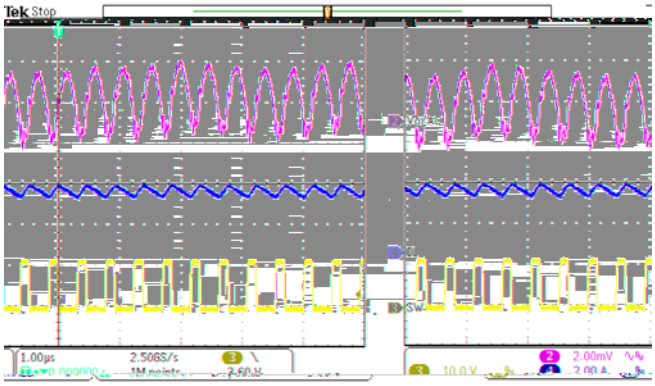

Figure 14. Buck1 Steady State (Io1 = 3A)

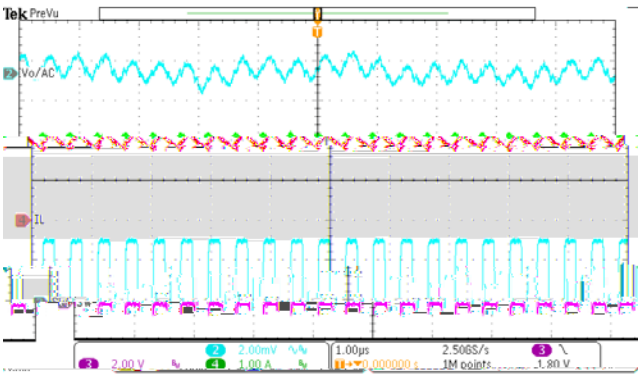

Figure 15. Buck2 Steady State (Io2 = 2A)

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Application Waveforms (continued)

Vin=12V, V_{OUT1}=3.3V, V_{OUT2}=1.1V, V_{OUT3}=1.5V, V_{OUT4}=5V, unless otherwise noted

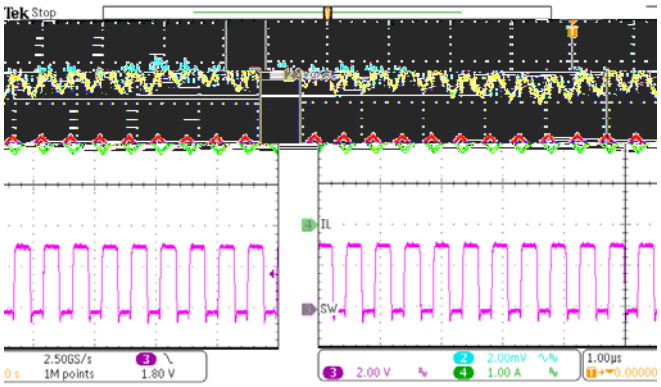

Figure 16. Buck3 Steady State (Io3 = 2A)

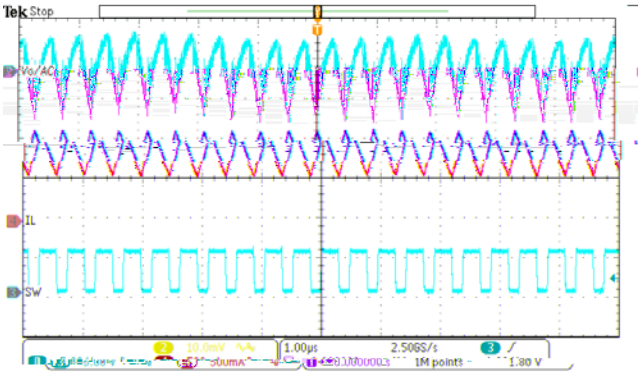

Figure 17. Boost4 Steady State (Io4 = 500mA)

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Layout Guideline

Proper PCB layout is a critical for device's stable and efficient operation. The traces conducting fast switching currents or voltages are easy to interact with stray inductance and parasitic capacitance to generate noise and degrade performance. For better results, follow these guidelines as below:

1. Power grounding scheme is very critical because of carrying power, thermal, and glitch/bouncing noise associated with clock frequency. The rule of thumb is to make ground trace lowest impendence and power are distributed evenly on PCB. Sufficiently placing ground area will optimize thermal and not causing over heat area.

2. Make sure the ground path between VIN capacitor and PGND1 pin is shortest with lowest impendence.

3. Place a low ESR ceramic capacitor as close to VIN and VIN23 pin and the ground as possible to reduce parasitic effect.

4. For operation at full rated load, the top side ground area must provide adequate heat dissipating area. Make sure top switching loop with power have lower impendence of grounding.

5. The bottom layer is a large ground plane connected to the ground plane on top layer by vias. The power pad should be connected to bottom PCB ground planes using multiple vias.

6. Output inductor should be placed close to the SW pin. The switching area of the PCB conductor minimized to prevent excessive capacitive coupling.

7. EN UVLO adjust resistors and feedback trace should connect to small signal ground which must return to the GND pin without any interleaving with power ground.

8. For achieving better thermal performance, a four-layer layout is strongly recommended.

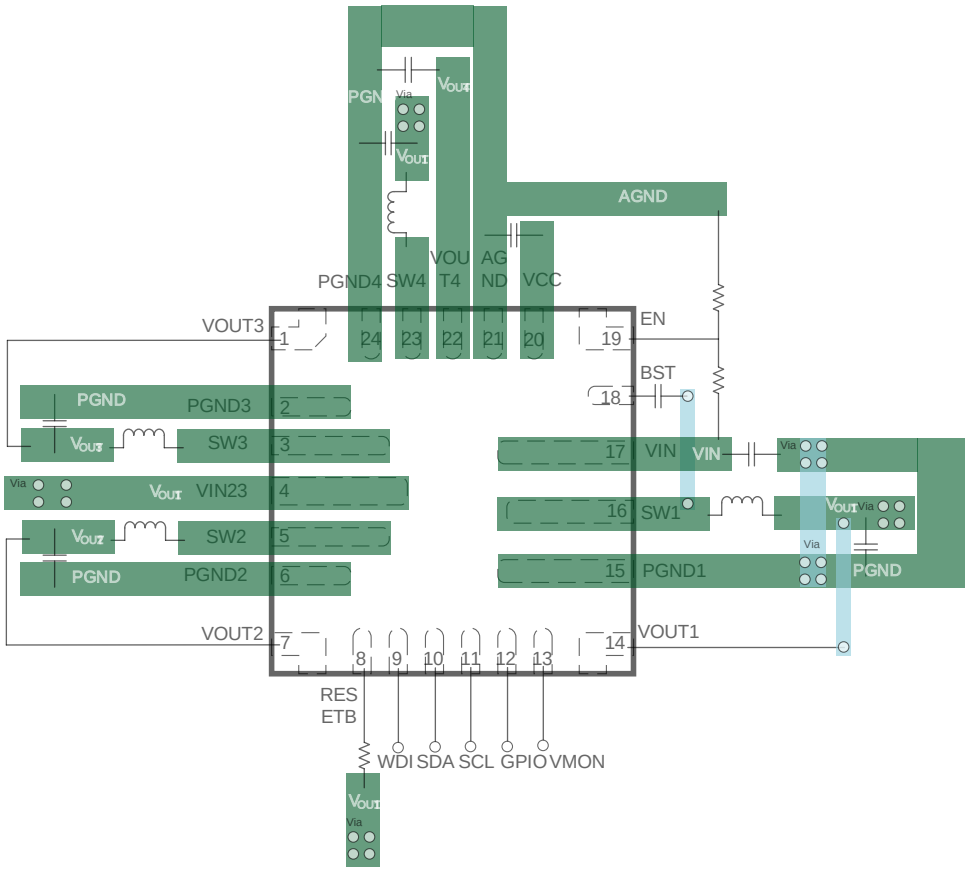

Figure 18. PCB Layout Example

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Register Map

ADDRESS	REGISTER	DEFAULT VALUE	OTP ACCESS	I2C LOCK	WD LOCK
0x00	CHIPID	-	Y	N	N
0x01	CONFIG_FSS	70h	Y	Y	N
0x02	CONFIG_T1	01h	Y	Y	N
0x03	CONFIG_T2	1Fh	Y	Y	N
0x05	CONFIG_EN	1Dh	Y	Y	N
0x06	CONFIG_PU1	32h	Y	Y	N
0x07	CONFIG_PU2	10h	Y	Y	N
0x08	RSTMAP	1Fh	Y	Y	N
0x0A	STATUV	00h	N	N	N
0x0B	STATOV	00h	N	N	N
0x0C	STATOFF	00h	N	N	N
0x0D	STATD	00h	N	N	N
0x0E	STATWD	00h	N	N	N
0x0F	VOUT2	06h	Y	Y	N
0x10	VOUT3	0Eh	Y	Y	N
0x11	CONFIG_MISC	60h	Y	Y	N
0x12	CONFIG_PFM	00h	Y	Y	N
0x13	CONFIG_WD1	87h	Y	N	Y
0x14	CONFIG_WD2	0Eh	Y	N	Y
0x15	CONFIG_WD3	13h	Y	N	Y
0x16	WD_KEY	AAh	Y	N	N
0x17	WD_LOCK	00h	N	N	N
0x19	CONFIG_PGSEL1	01h	Y	Y	N
0x1A	CONFIG_PGSEL2	55h	Y	Y	N
0x1C	I2C_LOCK	01h	N	N	N
0x22	SYS_STATE	00h	N	N	N

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CHIPID [7:0]				
ADDRESS: 0x00				
BITS	**FIELD**	**TYPE**	**DESCRIPTION**	**DECODE**
[7:6]	RESERVED	R	/	Reserved, always read as 01b
[5:0]	CONFIG_ID	W/R	Chip Configuration Identification. This is a unique number identifying the factory configuration of the device. This helps identify/verify the configuration without having to look at all configuration registers.	See Ordering Information

CONFIG_FSS [7:0]				
ADDRESS: 0x01				
BITS	**FIELD**	**TYPE**	**DESCRIPTION**	**DECODE**
[7]	EN_HOLD	W/R	Enable Hold. Overrides the EN pin to keep the device enabled. This bit is cleared when RESETB is asserted.	0 = EN pin controls power down 1 = Device enabled. Ignores EN pin state
[6]	FSS_EN	W/R	Frequency Spread Spectrum Enable.	0 = Disabled 1 = Enabled
[5]	FSS_MODE	W/R	Frequency Spread Spectrum Mode.	0 = Pseudorandom Modulation 1 = Triangle Modulation
[4]	FSS_PERIOD	W/R	Frequency Spread Period.	0 = 4.5KHz 1 = 10KHz
[3:2]	FSS_RANGE	W/R	Frequency Spread Spectrum Range.	00 = ±5%; 01 = ±2.5%; 10 = ±7.5%; 11 = ±3.75%
[1]	PMIC_RESET_EN	W/R	Enable PMIC reset Function. After this bit is set to 1, writing EN_ALL[0]=0 will shut down all power channels, reset all registers and restart automatically.	0 = Disabled 1 = Enabled
[0]	PEC_EN	W/R	Packet Error Checking Enable. Set this bit to a 1 to enable PEC or 0 to disable PEC.	0 = Disabled 1 = Enabled

CONFIG_T1 [7:0]				
ADDRESS: 0x02				
BITS	**FIELD**	**TYPE**	**DESCRIPTION**	**DECODE**
[7:6]	RESETB_HT	W/R	RESETB Hold Time Selection. This is the amount of time that the RESET pin is active (low) after the event that caused the RESET pin to activate is removed.	00 = 10ms; 01 = 20ms; 10 = 30ms; 11 = 40ms
[5:4]	RESETB_DLYR	W/R	RESETB Rising delay when state change from POWERUP to NORMAL	00 = 2.5ms; 01 = 5ms; 10 = 7.5ms; 11 = 10ms
[3:2]	RESERVED	R	/	/
[1:0]	DELAY_SCALE	W/R	Power up and Recover On Delay Scale.	00: Scale=0.5ms. Delay ranges from 0~7.5ms 01: Scale =1ms. Delay ranges from 0-

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				15ms 10: Scale=2.5ms. Delay ranges from 0-37.5ms 11: Scale =5ms. Delay ranges from 0-75ms

CONFIG_T2 [7:0]				
ADDRESS: 0x03				
BITS	**FIELD**	**TYPE**	**DESCRIPTION**	**DECODE**
[7:6]	RESERVED	R	/	/
[5]	DF_SCALE	W/R	OV/UV Digital Filter. Adds additional filtering to all OV/UV comparators.	Analog Filter Time = 10µs. Added Digital Filter Timeo! =DF[4:0] x 2µs, when DF_SCALE=0, =DF[4:0] x 10µs, when DF_SCALE=1.
[4:0]	DF	W/R		

CONFIG_EN [7:0]				
ADDRESS: 0x05				
BITS	**FIELD**	**TYPE**	**DESCRIPTION**	**DECODE**
[7:6]	RESERVED	R	/	/
[5]	EN_VMON	W/R	Enable for VMON. This bit will be activated every time entering DEEPSAFE state, don't change this bit in NORMAL state.	0 = VMON Disabled 1 = VMON Enabled
[4]	EN4	W/R	Enable for LV BOOST OUT4. This bit will be activated every time entering DEEPSAFE state, don't change this bit in NORMAL state.	0 = Output Disabled 1 = Output Enabled
[3]	EN3	W/R	Enable for LV BUCK OUT3. This bit will be activated every time entering DEEPSAFE state, don't change this bit in NORMAL state.	0 = Output Disabled 1 = Output Enabled
[2]	EN2	W/R	Enable for LV BUCK OUT2. This bit will be activated every time entering DEEPSAFE state, don't change this bit in NORMAL state.	0 = Output Disabled 1 = Output Enabled
[1]	RESERVED	R	/	/
[0]	EN_ALL	W/R	Enable for all channel	0 = Output Disabled 1 = Output Enabled

CONFIG_PU1 [7:0]				
ADDRESS: 0x06				
BITS	**FIELD**	**TYPE**	**DESCRIPTION**	**DECODE**

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				ON_DELAY4[3:0] x 1ms when DELAY_SCALE=10, t_{ON_DELAY4} = ON_DELAY4[3:0] x 2.5ms when DELAY_SCALE=11, t_{ON_DELAY4} = ON_DELAY4[3:0] x 5ms

CONFIG_PU2 [7:0]				
ADDRESS: 0x07				
BITS	**FIELD**	**TYPE**	**DESCRIPTION**	**DECODE**
[7:4]	ON_DELAY3	W/R	OUT3 Power-Up and Recover Turn On delay.	when DELAY_SCALE=00, t_{ON_DELAY3} = ON_DELAY3[3:0] x 0.5ms when DELAY_SCALE=01, t_{ON_DELAY3} = ON_DELAY3[3:0] x 1ms when DELAY_SCALE=10, t_{ON_DELAY3} = ON_DELAY3[3:0] x 2.5ms when DELAY_SCALE=11, t_{ON_DELAY3} = ON_DELAY3[3:0] x 5ms
[3:0]	ON_DELAY2	W/R	OUT2 Power-Up and Recover Turn On delay.	when DELAY_SCALE=00, t_{ON_DELAY2} = ON_DELAY2[3:0] x 0.5ms when DELAY_SCALE=01, t_{ON_DELAY2} = ON_DELAY2[3:0] x 1ms when DELAY_SCALE=10, t_{ON_DELAY2} = ON_DELAY2[3:0] x 2.5ms when DELAY_SCALE=11, t_{ON_DELAY2} = ON_DELAY2[3:0] x 5ms

RSTMAP [7:0]				
ADDRESS: 0x08				
BITS	**FIELD**	**TYPE**	**DESCRIPTION**	**DECODE**
[7:6]	RESERVED	R	/	/
[5]	RSTMAP_VMON	W/R	RESETB Pin Mapping for VMON.	0 = VMON OV and UV not mapped to RESETB pin 1 = VMON OV and UV are mapped to RESETB pin
[4]	RSTMAP_VO4	W/R	RESETB Pin Mapping for OUT4.	0 = OV[4] and UV[4] not mapped to RESETB pin 1 = OV[4] and UV[4] are mapped to RESETB pin
[3]	RSTMAP_VO3	W/R	RESETB Pin Mapping for OUT3.	0 = OV[3] and UV[3] not mapped to RESETB pin 1 = OV[3] and UV[3] are mapped to RESETB pin
[2]	RSTMAP_VO2	W/R	RESETB Pin Mapping for OUT2.	0 = OV[2] and UV[2] not mapped to RESETB pin 1 = OV[2] and UV[2] are mapped to RESETB pin
[1]	RSTMAP_VO1	W/R	RESETB Pin Mapping for OUT1.	0 = OV[1] and UV[1] not mapped to RESETB pin 1 = OV[1] and UV[1] are mapped to RESETB pin

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[0]	RSTMAP_WD	W/R	RESETB Pin Mapping for WD ERROR (WD_LFSR/ WD_UV/ WD_EXP)	0 = WD ERROR is not mapped to RESETB pin 1 = WD ERROR is mapped to RESETB pin

STATUV [7:0]				
ADDRESS: 0x0A				
BITS	**FIELD**	**TYPE**	**DESCRIPTION**	**DECODE**
[7]	UV	Read Clear	UV Comparator Status for all channels with Digital Filter.	0 = All enabled channels are above UV threshold after DF 1 = Any enabled channel is below UV threshold after DF
[6]	RESERVED	R	/	/
[5]	UV_VMON	Read Clear	UV warning for VMON Digital Filter is not included	0 = VMON is above UV threshold before DF 1 = VMON is below UV threshold before DF
[4]	UV_WAR4	Read Clear	UV warning for OUT4, Digital Filter is not included	0 = OUT4 is above UV threshold before DF 1 = OUT4 is below UV threshold before DF
[3]	UV_WAR3	Read Clear	UV warning for OUT3, Digital Filter is not included	0 = OUT3 is above UV threshold before DF 1 = OUT3 is below UV threshold before DF
[2]	UV_WAR2	Read Clear	UV warning for OUT2, Digital Filter is not included	0 = OUT2 is above UV threshold before DF 1 = OUT2 is below UV threshold before DF
[1]	UV_WAR1	Read Clear	UV warning for OUT1, Digital Filter is not included	0 = OUT1 is above UV threshold before DF 1 = OUT1 is below UV threshold before DF
[0]	RESERVED	R	/	/

STATOV [7:0]				
ADDRESS: 0x0B				
BITS	**FIELD**	**TYPE**	**DESCRIPTION**	**DECODE**
[7]	OV	Read Clear	OV Comparator Status for all channels with Digital Filter.	0 = All enabled channels are below OV threshold after DF 1 = Any enabled channel is above OV threshold after DF
[6]	RESERVED	R	/	/
[5]	OV_VMON	Read Clear	OV warning for VMON, Digital Filter is not included	0 = VMON is below OV threshold before DF 1 = VMON is above OV threshold before DF
[4]	OV_WAR4	Read Clear	OV warning for OUT4, Digital Filter is not included	0 = OUT4 is below OV threshold before DF 1 = OUT4 is above OV threshold before DF

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[3]	OV_WAR3	Read Clear	OV warning for OUT3, Digital Filter is not included	0 = OUT3 is below OV threshold before DF 1 = OUT3 is above OV threshold before DF
[2]	OV_WAR2	Read Clear	OV warning for OUT2, Digital Filter is not included	0 = OUT2 is below OV threshold before DF 1 = OUT2 is above OV threshold before DF
[1]	OV_WAR1	Read Clear	OV warning for OUT1, Digital Filter is not included	0 = OUT1 is below OV threshold before DF 1 = OUT1 is above OV threshold before DF
[0]	RESERVED	R	/	/

STATOFF [7:0]				
ADDRESS: 0x0C				
BITS	**FIELD**	**TYPE**	**DESCRIPTION**	**DECODE**
[7:5]	RESERVED	R	/	/
[4]	OFF4	Read Clear	OFF Comparator Status for OUT4	0 = OUT4 is above OFF threshold 1 = OUT4 is below OFF threshold
[3]	OFF3	Read Clear	OFF Comparator Status for OUT3	0 = OUT3 is above OFF threshold 1 = OUT3 is below OFF threshold
[2]	OFF2	Read Clear	OFF Comparator Status for OUT2	0 = OUT2 is above OFF threshold 1 = OUT2 is below OFF threshold
[1]	OFF1	Read Clear	OFF Comparator Status for OUT1	0 = OUT1 is above OFF threshold 1 = OUT1 is below OFF threshold
[0]	RESERVED	R	/	/

STATD [7:0]				
ADDRESS: 0x0D				
BITS	**FIELD**	**TYPE**	**DESCRIPTION**	**DECODE**
[7]	RESERVED	R	/	/
[6]	CLK_ERR	Read Clear	CLK fault indicator	0 = No fault detected 1 = CLK error detected
[5]	SUP_ERR	Read Clear	Supply fault indicator, include VCC OV fault and VIN OV fault	0 = No fault detected 1 = VCC OV or VIN OV detected
[4]	RST_ENTER	Read Clear	RESET state indicator	0 = No fault detected 1 = RESET state has entered since the last read.
[3]	DEEPSAFE_ENTER	Read Clear	DEEPSAFE state indicator	0 = No fault detected 1 = DEEPSAFE state has entered since the last read.
[2]	PIN_ERR	Read Clear	Pin fault indicator, include RESETB Pin stuck fault and GND pin LOSS fault	0 = No fault detected 1 = RESETB Short to supply detected or pull-down fail or GND LOSS since the last read
[1]	THSD	Read Clear	Thermal Shutdown Indication	0 = No thermal shutdown 1 = Thermal shutdown has occurred since last read
[0]	INTERR	Read Clear	Internal Error, include OTP CRC failure, LBIST and ABIST failure	0 = No internal error detected 1 = Internal error detected

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STATWD [7:0]				
ADDRESS: 0x0E				
BITS	**FIELD**	**TYPE**	**DESCRIPTION**	**DECODE**
[7:6]	RESERVED	R	/	/
[5]	RESETB_STAT	R	RESETB Pin State. Allows verification of the state of the RESETB pin. This is the real-time RESETB pin state.	0 = RESETB is low 1 = RESETB is high
[4]	WD_OPEN	R	Watchdog Open Window. This bit indicates that it is permissible to update the watchdog. This bit shows real-time status.	0 = Watchdog update not open 1 = Watchdog ok to update
[3]	WD_ERR	R	Watchdog ERROR for 1 time or 2 times (config by WD_FAIL_CNT), LFSR mismatch is not included	0 = No error detected 1 = Error detected
[2]	WD_LFSR	Read Clear	LFSR Write Mismatch. The MCU/SoC did not write the correct value to the WDKEY register.	0 = LFSR key match 1 = LFSR key mismatch since last read
[1]	WD_UV	Read Clear	Watchdog Update Violation. The MCU/SoC wrote to the WDKEY register during the CLOSE window.	0 = No violation detected 1 = Watchdog updated too early
[0]	WD_EXP	Read Clear	Watchdog Open Window Expired. The MCU/SoC did not write to the WDKEY register during the whole window.	0 = Watchdog timer not expired 1 = Watchdog timer expired

VOUT2 [7:0]				
ADDRESS: 0x0F				
BITS	**FIELD**	**TYPE**	**DESCRIPTION**	**DECO 557.04 395.04 0.96 0.96 re9.04 0**

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[4]	VIN_OVP_EN	W/R	Enable of VIN OVP. When VIN>43V, part enter DEEPSAFE mode.	0 = Disabled 1 = Enabled
[3:2]	VIN_START	W/R	VIN start threshold at VIN rising	00 = 3.2V; 01 = 4V; 10 = 5V; 11 = 6V
[1:0]	VIN_STOP	W/R	VIN stop threshold at VIN falling	00 = 2.8V; 01 = 3.5V; 10 = 4.5V; 11 = 5.5V

CONFIG_PFM [7:0]				
ADDRESS: 0x12				
BITS	**FIELD**	**TYPE**	**DESCRIPTION**	**DECODE**
[7:4]	RESERVED	R	/	/
[3]	PFM4	W/R	BOOST4 FCCM/PFM mode selection when NORMAL mode.	0 = FCCM 1 = PFM
[2]	PFM3	W/R	BUCK3 FCCM/PFM mode selection when NORMAL mode.	0 = FCCM 1 = PFM
[1]	PFM2	W/R	BUCK2 FCCM/PFM mode selection when NORMAL mode.	0 = FCCM 1 = PFM
[0]	PFM1	W/R	BUCK1 FCCM/PFM mode selection when NORMAL mode.	0 = FCCM 1 = PFM

CONFIG_WD1 [7:0]				
ADDRESS: 0x13				
BITS	**FIELD**	**TYPE**	**DESCRIPTION**	**DECODE**
[7]	WD_MODE	W/R	Simple Windowed Watchdog Enable	0 = QA watchdog enabled 1 = Simple watchdog enabled
[6]	WD_SCALE	W/R	Watchdog Clock Divider Scale	0 = 128μs 1 = 128μs x 64
[5:0]	WD_CLK	W/R	Watchdog Clock Divider	tWDCLK = (WD_CLK[5:0]+1) x WD_SCALE

CONFIG_WD2 [7:0]				
ADDRESS: 0x14				
BITS	**FIELD**	**TYPE**	**DESCRIPTION**	**DECODE**
[7:4]	WD_TCLOSE	W/R	Watchdog Close Window Duration Time. Sets the number of watchdog clock cycles before the open window starts.	tWD_CLOSE = tWDCLK x (WD_ TCLOSE [3:0]+1) x 8
[3:0]	WD_TOPEN	W/R	Watchdog Open Window Duration Time. Sets the number of watchdog clock cycles after the close window finishes.	tWD_OPEN = tWDCLK x (WD_ TOPEN[3:0]+1) x 8

CONFIG_WD3 [7:0]				
ADDRESS: 0x15				
BITS	**FIELD**	**TYPE**	**DESCRIPTION**	**DECODE**
[7:5]	RESERVED	R	/	/
[4]	WD_FAIL_CNT	W/R	Watchdog Failure counter config. When Watchdog failure times reach	0 = 1 time 1 = 2 times

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			the counter, report to RESETB and status register.	
[3]	WD_EN	W/R	Watchdog Enable	0 = Disabled 1 = Enabled
[2:0]	WD_1UD	W/R	First Update Extension. Sets the number of extra watchdog window cycles after POR to the normal watchdog window.	t1STWD_CLOSE = tWD_CLOSE x (WD_1UD [2:0] + 1) t1STWD_OPEN = tWD_OPEN x (WD_1UD [2:0] + 1)

WD_KEY [7:0]				
ADDRESS: 0x16				
BITS	**FIELD**	**TYPE**	**DESCRIPTION**	**DECODE**
[7:0]	WD_KEY	W/R	Watchdog Key.	The current key can be read from this register. To update the watchdog, the next value in the sequence must be written to this register. If configured as a simple windowed watchdog, writing any value to the WDKEY register will refresh the watchdog and the value written will be ignored. If configured as a QA watchdog, writing the incorrect response to the WDKEY register will result in the value written being ignored and a WD_LFSR violation. Writing the correct response in QA mode during an open window will result in a refresh and the WDKEY register being updated. Writing the correct response in QA mode during a closed window will result in the write being ignored and a WD_UV violation. LFSR polynomial: x8 + x6 + x5 + x4 + 1

WD_LOCK [7:0]				
ADDRESS: 0x17				
BITS	**FIELD**	**TYPE**	**DESCRIPTION**	**DECODE**

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[1:0]	PGVMON_SEL	W/R	VMON OV/UV threshold selection.	00 = Reserved; 01 = ±6%; 10 = ±8%; 11 = ±10%

CONFIG_PGSEL2 [7:0]				
ADDRESS: 0x1A				
BITS	**FIELD**	**TYPE**	**DESCRIPTION**	**DECODE**
[7:6]	PG4_SEL	W/R	OUT4 OV/UV threshold selection.	00 = Reserved; 01 = ±6%; 10 = ±8%; 11 = ±10%
[5:4]	PG3_SEL	W/R	OUT3 OV/UV threshold selection.	00 = Reserved; 01 = ±6%; 10 = ±8%; 11 = ±10%
[3:2]	PG2_SEL	W/R	OUT2 OV/UV threshold selection.	00 = Reserved; 01 = ±6%; 10 = ±8%; 11 = ±10%
[1:0]	PG1_SEL	W/R	OUT1 OV/UV threshold selection.	00 = Reserved; 01 = ±6%; 10 = ±8%; 11 = ±10%

I2C_LOCK [7:0]				
ADDRESS: 0x1C				
BITS	**FIELD**	**TYPE**	**DESCRIPTION**	**DECODE**
[7:1]	RESERVED	R	/	/

[0] I2C_LOCK](2C)-1.6MCID 42 46

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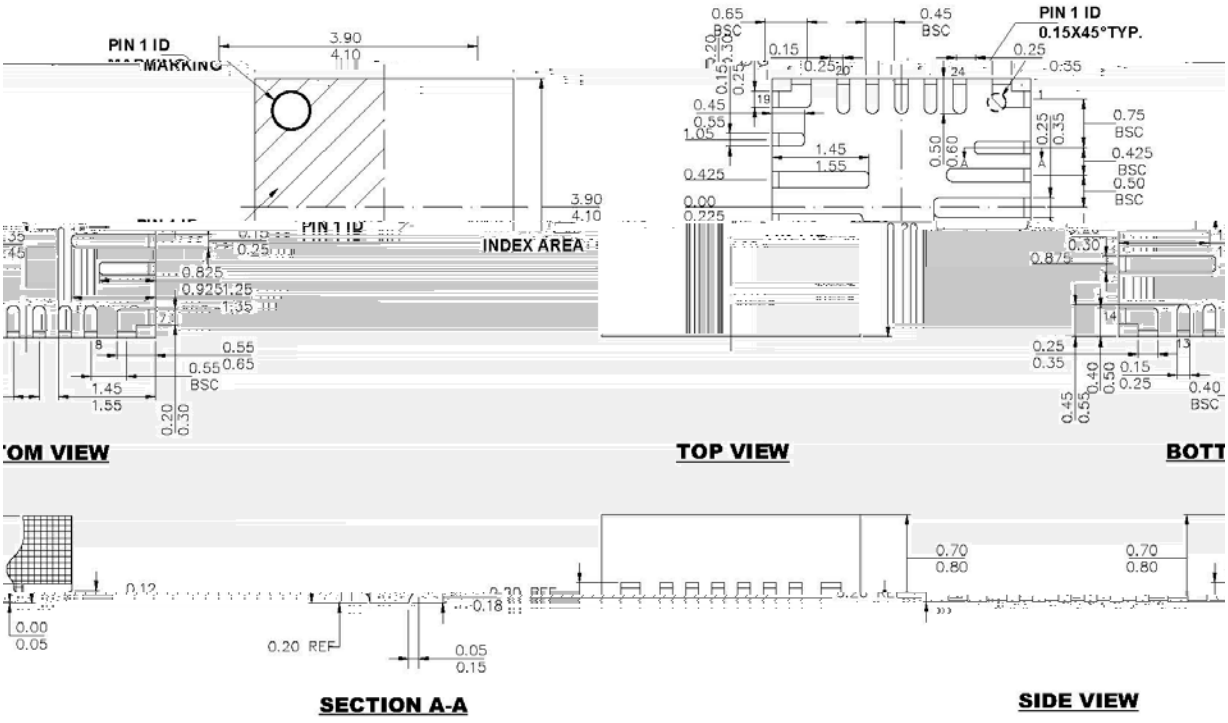
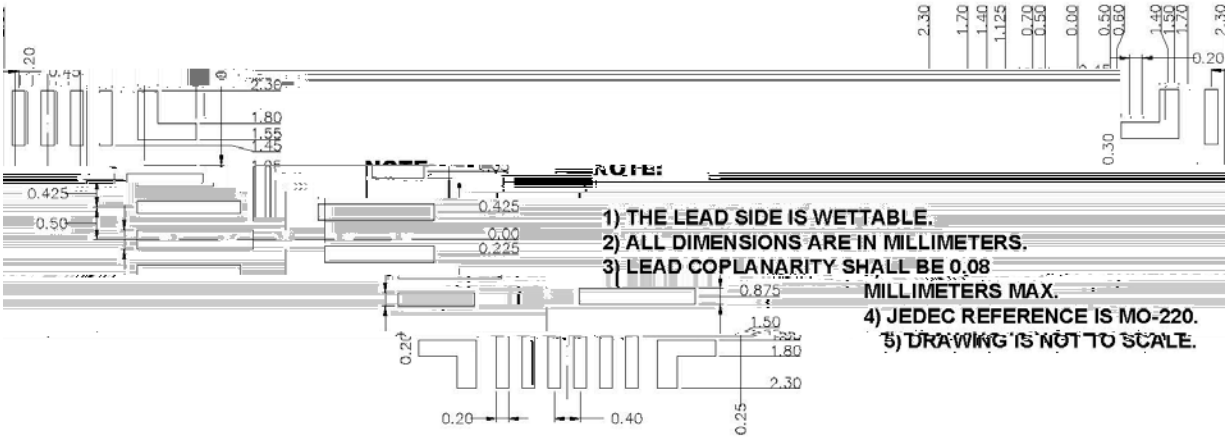
PACKAGE INFORMATION





RECOMMENDED LAND PATTERN

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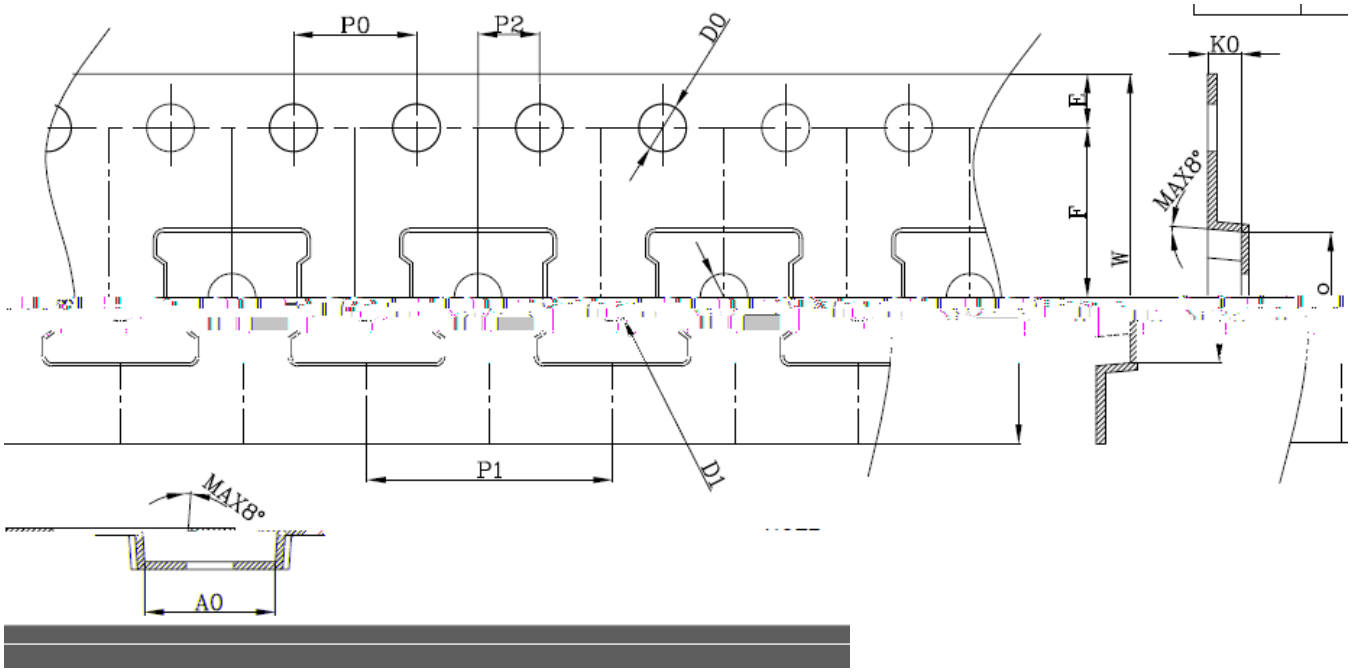

SYMBOL	A0	B0	K0	P0	P1	P2
±0.10	8.00±0.10	2.00±0.05	SPEC	4.30±0.10	4.30±0.10	1.10±0.10
D0	D1	W	SYMBOL	T	E	F
±0.05	1.55±0.10	12.00±0.30	SPEC	0.30±0.05	1.75±0.10	5.50±0.05

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